Digital Circuit Design
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Lecture #1

Introduction, Logic Circuits

Administrative

Handouts

- Course Syllabus (readings due **before** lecture)
  http://DoctorD.WebHop.net
- Linked Resources on Syllabus

Grading

- 20% Homework (Due the week following the lecture on that topic)
- 2 midterms (40%) + cumulative final (40%)
- all exams required; make arrangements in advance if you have a conflict.
- Lab Note: You should prepare prior to Lab session
  - Paper design (if required)
  - Functioning simulation

Number Systems

Radix 10 Why? (0, 1, 9)

$5{,}273 = 5*10^3 + 2*10^2 + 7*10^1 + 3*10^0$

Binary Radix 2 (0,1)

On/off

$153 = 2^7 + 2^3 + 2^0 = 10001001$

Octal Radix 8 (0, 1, 7)

$153 = 2*8^2 + 3*8^1 + 8^0 = 231$

Hexadecimal Radix 16 (0, 1, 9, A, F)

$153 = 9*16^1 + 9*16^0 = 99$

Complements

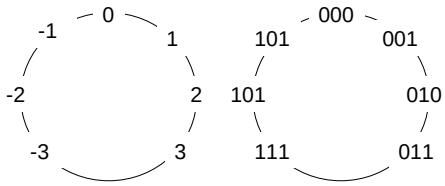
(Representing Negative Numbers)

Signed-magnitude Binary

9 = 00001001

Sign bit

-9 = 10001001

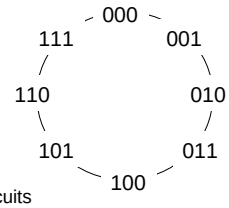


1 s complement (complement all bits)

-9 = 11110110

2 s complement (add 1 to the 1 s complement)

-9 = 11110111



Illustrative Example: 9 s Complement

Decimal Subtraction

```
  575
- 57
  518
```

9 s Complement

-057 = 942

```
  575
 1517
```

now wrap the overflow around and add for the answer

518

10 s Complement

-057 = 942+1 = 943

```
  575
 1518
```

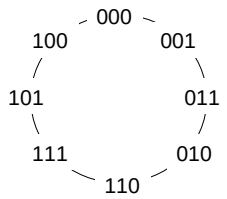
Here ignore the overflow to get 518

Other Codes

BCD (10, 4-bit binary codes per digit)

Gray Code

only one bit changes between adjacent Digits



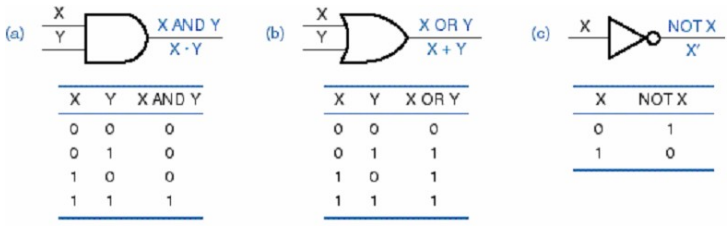
ASCII

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NUL	SOH	STX	ETX	EOT	ENQ	ACK	BEL	BS	HT	LF	VT	FF	CR	SO	SI
1	DLE	DC1	DC2	DC3	DC4	NAK	SYN	ETB	CAN	EM	SUB	ESC	FS	GS	RS	US
2	SP	!	"	#	$	%	&	'	(	)	*	+	,	-	.	/
3	0	1	2	3	4	5	6	7	8	9	:	;	<	=	>	?
4	@	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
5	P	Q	R	S	T	U	V	W	X	Y	Z	[	\	]	^	_
6	`	a	b	c	d	e	f	g	h	I	j	k	l	m	n	o
7	p	q	r	s	t	u	v	w	x	y	z	{	|	}	~	DEL

Digital Logic

Binary system -- 0 & 1, LOW & HIGH, negated and asserted.

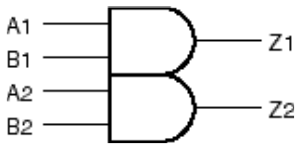
Basic building blocks -- AND, OR, NOT



X	Y	X AND Y
0	0	0
0	1	0
1	0	0
1	1	1

X	Y	X OR Y
0	0	0
0	1	1
1	0	1
1	1	1

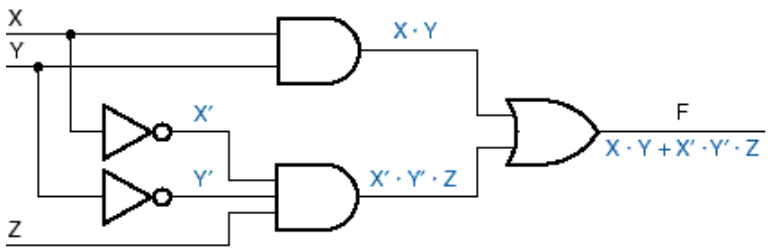
X	NOT X
0	1
1	0



Digital Logic Continued

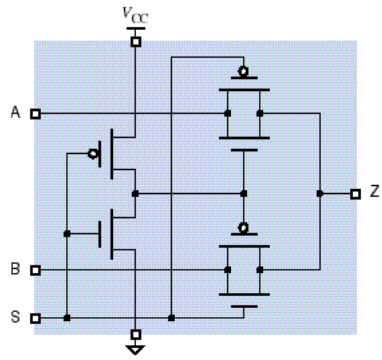
X	Y	X NAND Y
0	0	1
0	1	1
1	0	1
1	1	0

X	Y	X NOR Y
0	0	1
0	1	0
1	0	0
1	1	0



Many representations of digital logic

Transistor-level circuit diagrams

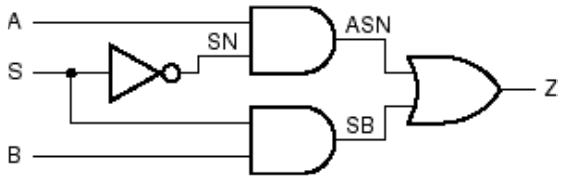


Gate symbols (for simple elements)

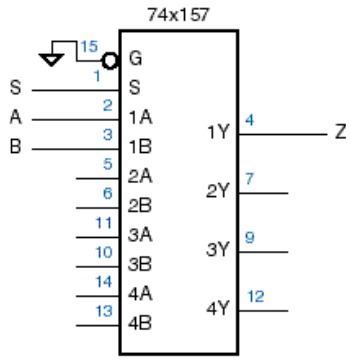
Truth tables

S	A	B	Z
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

Logic diagrams



Prepackaged building blocks, e.g. multiplexer



Equations: $Z = S' \cdot A + S \cdot B$

Various hardware description languages

ABEL

```
module chap1mux
title 'Two-input multiplexer example'
CHAP1MUX device 'P16V8'

A, B, S      pin 1, 2, 3;
Z            pin 13 istype 'com';

equations

WHEN S == 0 THEN Z = A;  ELSE Z = B;

end chap1mux
```

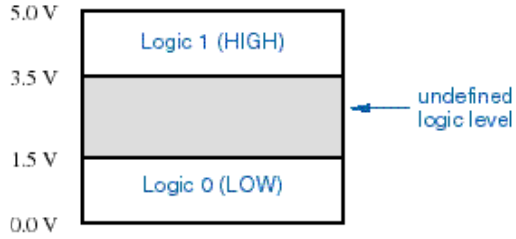
VHDL

```
library IEEE;
use IEEE.std_logic_1164.all;

entity Vchap1mux is
    port ( A, B, S: in  STD_LOGIC;
           Z:       out STD_LOGIC );
end Vchap1mux;

architecture Vchap1mux_arch of Vchap1mux is
begin
  Z <= A when S = '0' else B;
end Vchap1mux_arch;
```

We ll start with gates and work our way up

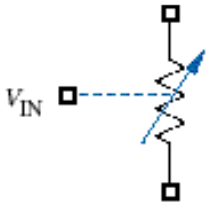
Logic levels

- Undefined region is inherent
  - digital, not analog
  - amplification, weak => strong



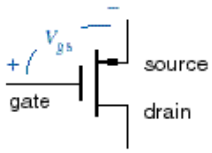
- Switching threshold varies with voltage, temp, process, phase of the moon
  - need noise margin
- The more you push the technology, the more analog it becomes.
- Logic voltage levels decreasing with process
  - 5 -> 3.3 -> 2.5 -> 1.8 V

MOS Transistors



Voltage-controlled resistance

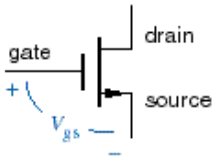
PMOS



Voltage-controlled resistance: decrease V_{gs} ==> decrease R_{ds}

Note: normally, $V_{gs} \leq 0$

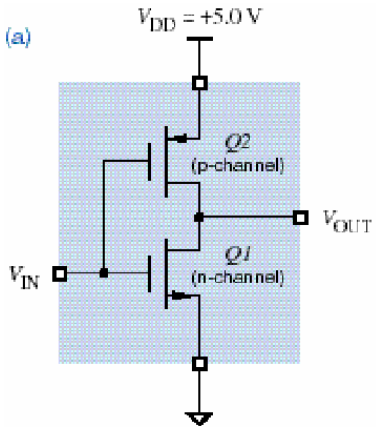
NMOS



Voltage-controlled resistance: increase V_{gs} ==> decrease R_{ds}

Note: normally, $V_{gs} \geq 0$

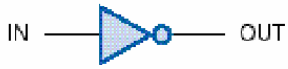
CMOS Inverter



(b)

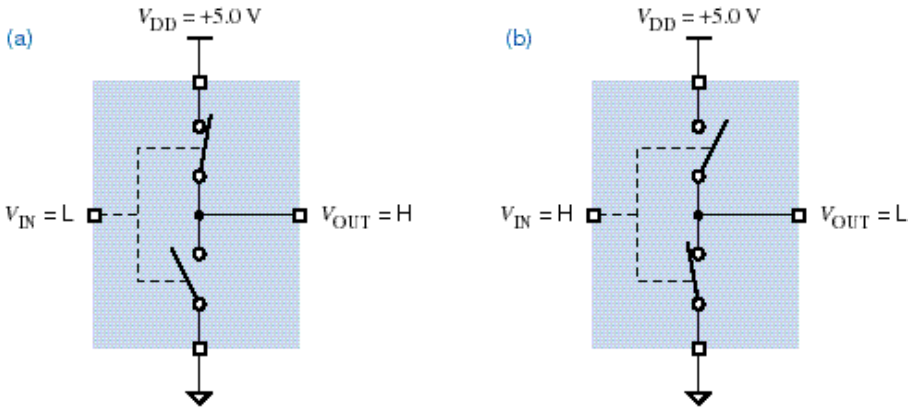
V_{IN}	Q1	Q2	V_{OUT}
0.0 (L)	off	on	5.0 (H)
5.0 (H)	on	off	0.0 (L)

(c)



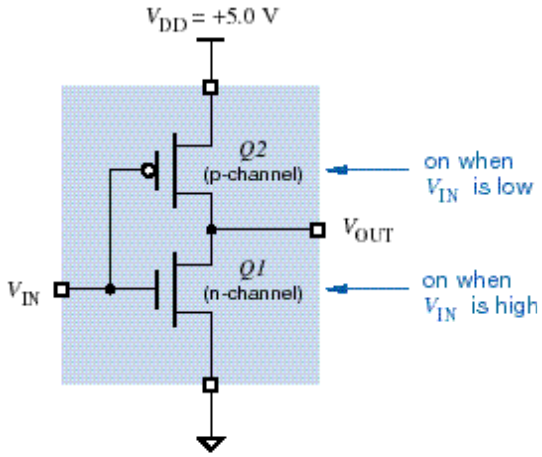
Switch model

Simplified Inverter Model



Alternate transistor symbols

Inverter Again



CMOS Gate Characteristics

No DC current flow into MOS gate terminal

- However gate has capacitance ==> current required for switching (CV^2f power)

No current in output structure, except during switching

- Both transistors partially on
- Power consumption related to frequency
- Slow input-signal rise times ==> more power

Symmetric output structure ==> equally strong drive in LOW and HIGH states