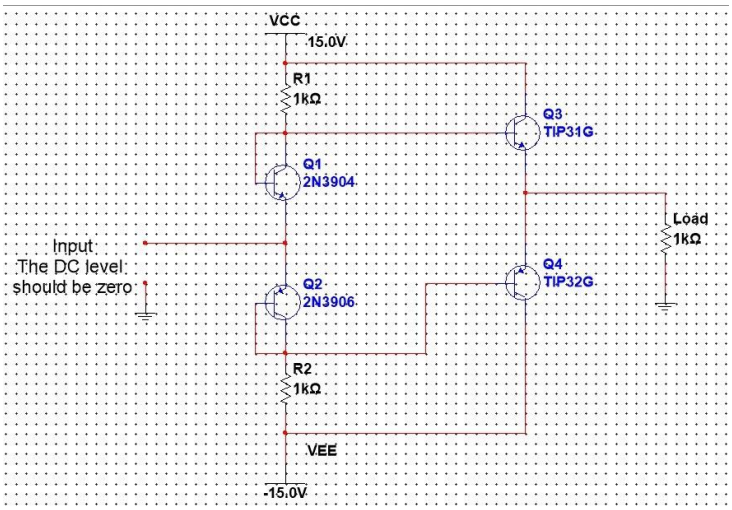

Designing an A-B Amplifier Stage

Introduction: Amplifier Classes

Al of the amplifiers we have discussed so far are class "A" amplifiers. This means that the active device is biased to be in a conducting state for the full peak to peak cycle of the signal. There are other classes:

- **Class "B"** – where each device only conducts for ½ of the signal cycle. Therefore, there has to be two devices, each device handles either the positive signal cycle or the negative signal cycle. These amplifiers are more efficient in operation than the Class "A" amplifier. Care needs to be taken to make sure that there is a clean handoff of the signal as responsibility shifts at zero crossings or you get "Crossover Distortion".
- **Class "A-B"** – Which we will focus on in this lab as a power output stage. Here the crossover problem is minimized by allowing an overlap (both devices still operate) between the devices as the zero crossing occurs. There is a minor sacrifice of amplifier efficiency compared to a pure class "B" amplifier.
- **Class "C"** – where the amplifier device only conducts during positive peaks. This is a non-linear amplifier used for RF power stages and are followed by a filter to only pass the desired frequency (Block the harmonics). Class "C" amplifiers are more efficient than any of the above amplifiers.
- **Class "D"** - A class-D amplifier or switching amplifier is an electronic amplifier in which the amplifying devices (transistors, usually MOSFETs) operate as electronic switches, and not as linear gain devices as in other amplifiers. These are even more efficient than any of the others but have limitations in how high a signal frequency they can handle. Powered subwoofers often use class "D" amplifiers.

A class A-B Amplifier stage

Below is a prototype Push-Pull class A-B amplifier (again I have left the sizing of the resistors to you)

Q3 is a power NPN transistor to handle positive output portions of the signal

Q4 is a power PNP transistor to handle negative output portions of the signal

Q1 and Q2 provide a diode drops to offset DC levels and properly bias the power transistors as described in your textbook

Note: this design relies on the matching between the NPN and PNP transistors (they are not quite a match) to get a 0 DC offset in the signal output with a 0 DC offset in the input signal. The gain should be almost unity since each output transistor is effectively an emitter follower when active.