Review for Quiz 7

Part 7f of
"Electronics and Telecommunications"
A Fairfield University E-Course
Powered by LearnLinc

Module: Digital Electronics
(in two parts)

- Text: "Digital Logic Tutorial ," Ken Bigelow, http://www.play-hookey.com/digital/
- References:
  - "Electronics Tutorial", part 10 (Thanks to Alex Pounds) http://doctord.dyndns.org:8000/courses/Topics/Electronics/Alex_Pounds/Index.htm
- Contents:
  - 7 – Digital Electronics 1
    - 5 on-line sessions plus one lab and a quiz
  - 8 – Digital Electronics 2
    - 5 on-line sessions plus one lab and a quiz
- Mastery Test part 4 follows this Module

Section 7: Digital Electronics 1

- Logic gates and Boolean algebra
- Truth Tables
- Binary numbers
- Memory
- Flip-Flops

Section 8: Digital Electronics 2

- Clocks and Counters
- Shift Registers
- Decoders
- Multiplexers & Demultiplexers
- Sampling

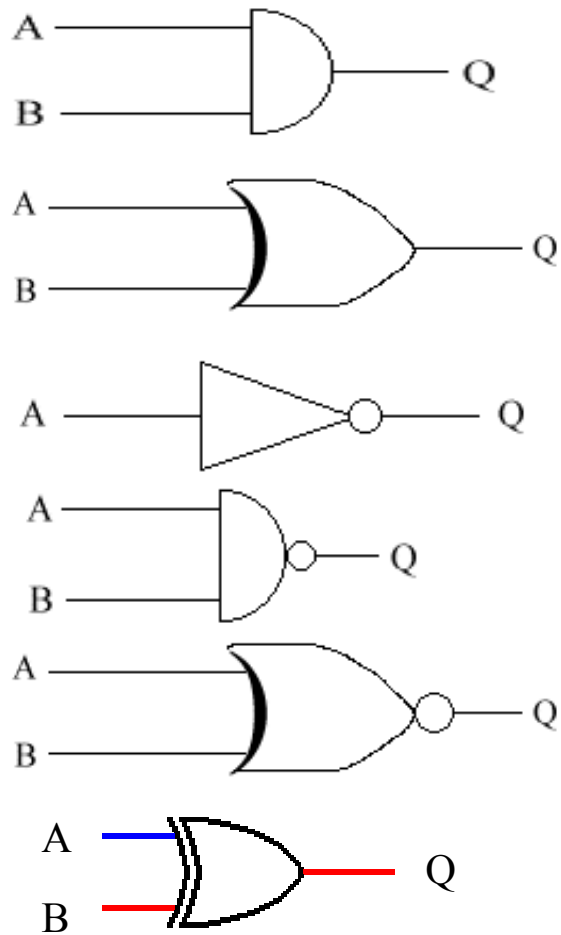
- **MT4**

Section 7 Schedule

Session 7a	03/05	Introduction: Binary, Logic Gates and Boolean	Alex Pounds: Part 10 “Ken B”: Home, Basic Gates, & Boolean Algebra
Session 7b	03/10	Logic Gates and Truth Tables	Alex Pounds: Part 10 “Ken B”: Derived Gates, Xor
Session 7c	03/12	Binary numbers	“Keb B”: Binary Addition “Vinay “: Binary Numbers
Session 7d	03/17	Memory: The Latch, Registers, RAM & ROM	“Ken B”: RS Nand Latch, Clocked RS Latch, D Latch
Session 7e (Lab - 03/22, Sat.)	03/19	Pulses, Clocks and Flip-Flops	“Ken B”: RS Flip-Flop, JK Flip-Flop, D Flip-Flop, Flip-Flop Symbols
Session 7f (Quiz 7 due 03/30)	**03/24**	**Review for Quiz 7**	
Session 7g	03/31	Quiz Results	

Basics

- Binary: 1, 0; True, False; On, Off; High, Low; 5 volts, 0 volts
- Basic Logic Gates:
  - AND: Q = A * B * C
    (Q is only true if all inputs are true)
  - OR: Q = A +B + C
    (Q is only false if all inputs are false)
  - NOT: Z = X′
    (Q is true if A is false, Q is false if A is true)
- Derived Logic Gates:
  - NAND
    (Q is only false if all inputs are true)
  - NOR
    (Q is only true if all inputs are false)
  - XOR
    (Q is true if one of A or B is true but not both)



Truth Tables

- Truth Tables: Enumerate outputs for all input combinations
  - Example: 5 people are voting for one of two candidates
    Let 0 represent Candidate A and 1 represent candidate B

Voter1	Voter2	Voter3	Winner
0	0	0	A
0	0	1	A
0	1	0	A
0	1	1	B
1	0	0	A
1	0	1	B
1	1	0	B
1	1	1	B

Boolean Algebra

- Named Variables
- Operators
- Expressions
- Equations
- Rules

(T1)	$X + 0 = X$	(T1′)	$X \cdot 1 = X$	(Identities)
(T2)	$X + 1 = 1$	(T2′)	$X \cdot 0 = 0$	(Null elements)
(T3)	$X + X = X$	(T3′)	$X \cdot X = X$	(Idempotency)
(T4)	$(X')' = X$			(Involution)
(T5)	$X + X' = 1$	(T5′)	$X \cdot X' = 0$	(Complements)

(T6)	$X + Y = Y + X$	(T6′)	$X \cdot Y = Y \cdot X$	(Commutativity)
(T7)	$(X + Y) + Z = X + (Y + Z)$	(T7′)	$(X \cdot Y) \cdot Z = X \cdot (Y \cdot Z)$	(Associativity)
(T8)	$X \cdot Y + X \cdot Z = X \cdot (Y + Z)$	(T8′)	$(X + Y) \cdot (X + Z) = X + Y \cdot Z$	(Distributivity)
(T9)	$X + X \cdot Y = X$	(T9′)	$X \cdot (X + Y) = X$	(Covering)
(T10)	$X \cdot Y + X \cdot Y' = X$	(T10′)	$(X + Y) \cdot (X + Y') = X$	(Combining)
(T11)	$X \cdot Y + X' \cdot Z + Y \cdot Z = X \cdot Y + X' \cdot Z$			(Consensus)
(T11′)	$(X + Y) \cdot (X' + Z) \cdot (Y + Z) = (X + Y) \cdot (X' + Z)$			

Binary Numbers:

- Based on powers of 2

  0 1 1 0 1 1 0 1 = 64 + 32 + 8 + 4 + 1 = 109

  128 64 32 16 8 4 2 1

- k bits can count up to $2^k - 1$ (2^k values including zero)
  - 8-bits ⇨ 256 values, 16-bits ⇨ 65536 values (64k binary)
  - 10-bits ⇨ 1024 values (1k binary)
  - 20-bits ⇨ 1,048,576 values (1 meg binary)
  - Bits, Nibbles (4), Bytes (8), and Words
  - Negative Numbers: Two's complement
  - Binary Adders: half and full

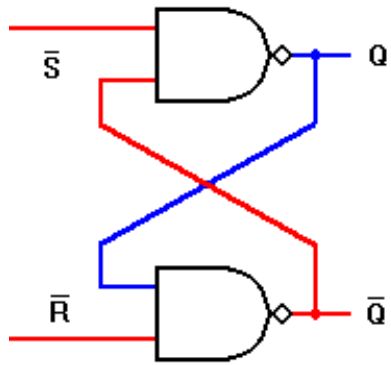
    0 1 1 0 1 1 0 1 = 109

    +0 0 0 0 1 0 1 1 = 11

    0 1 1 1 1 0 0 0 = 120

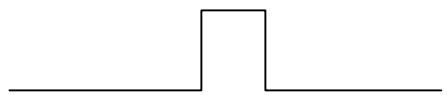
Storage

- The RS Latch (a "bit" of storage)
  - Set = 1: Q=1
  - Reset = 1: Q=0
- Register (n-bits of storage)
  - n latches (or flip-flops)
  - Stores a word (or byte) of data
- RAM (addressable words of memory)
  - Read / write
  - Volatile (data lost if power lost)
- ROMs, PROMs, EPROMs and EEROMS
  - Non-volatile memories

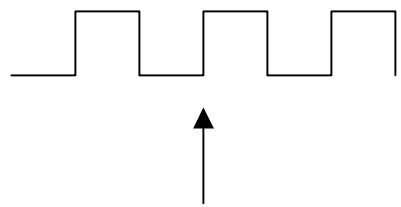


Pulses and Clocks

- Single Pulse
  - Signal normally low then high for a short time and goes back to low



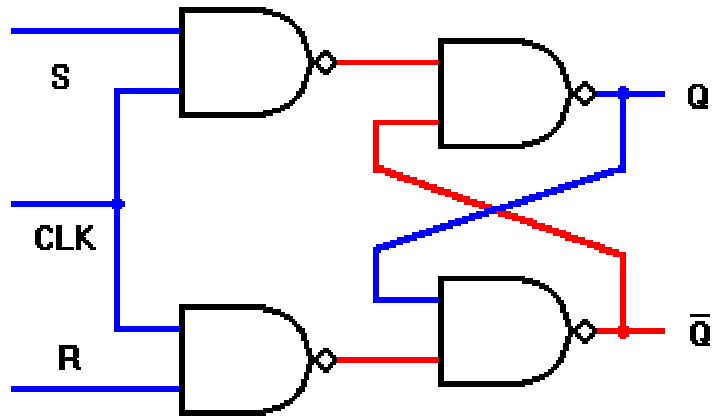
- Clock
  - Signal alternates high-low at a regular rate



Positive going edge

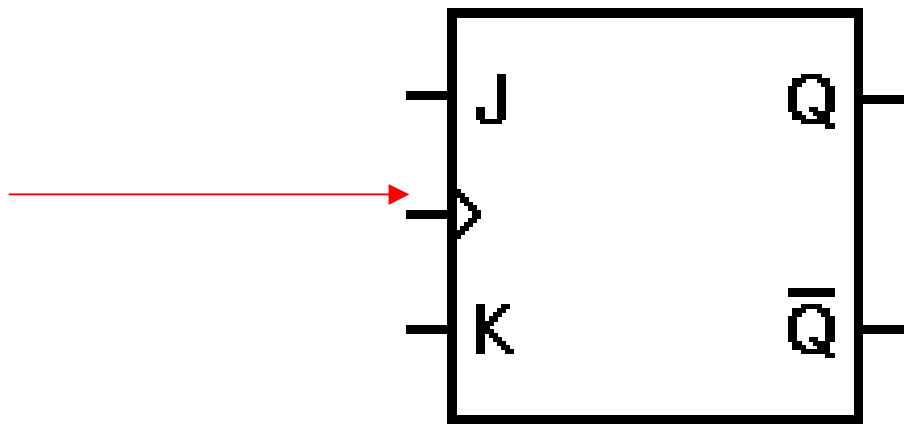
Clocked Logic

- Clock signal “enables Set and Reset pins
- Synchronous Logic
  - Slower than “ripple” logic
    - Gates have input to output “delay”
    - Delays build up as signals propagate through the logic
  - Predictable timing
    - Clocked (synchronous) logic prevents the build up of delays



The JK Flip-Flop

- Edge Triggered Generic Flip-Flop
  - the triangle symbol
    - triangle: rising edge triggers change
    - Not then triangle: falling edge triggers change
- Truth Table
  - J and K determines state change



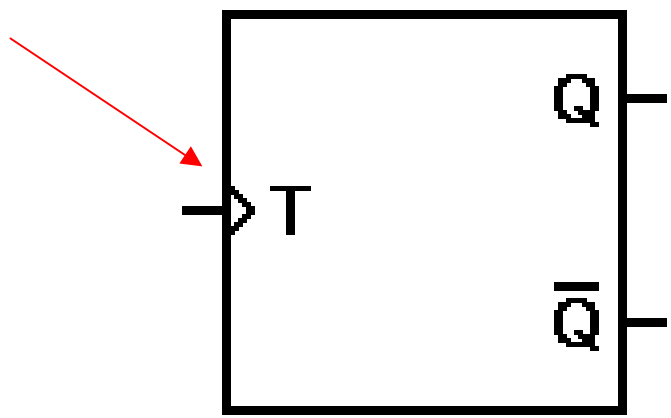
J	K	Q(t+1)
0	0	Q(t) – No change
0	1	0 – Reset
1	0	1 – Set
1	1	Q′(t) – Complement

The T Flip-Flop

- State toggles (flips) on each positive going clock edge

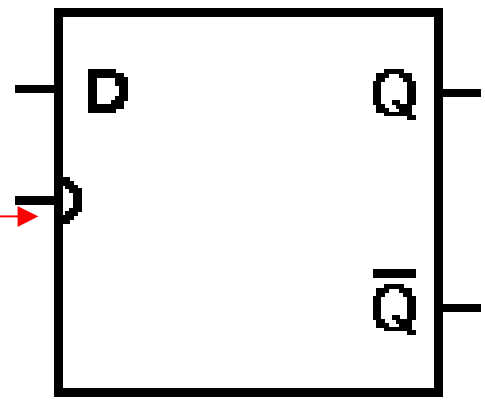
Triangle: edge triggered

T	Q(t+1)
0	Q(t) – No change
1	Q′(t) - Complement



The D Flip-Flop

- Simple triggered storage Flip-Flop
  - Note the half circle
  - It is controlled by clock level, not an edge



D	Q(t+1)
0	0 - Reset
1	1 - Set

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