Clocks and Counters

Part 8a of
"Electronics and Telecommunications"
A Fairfield University E-Course
Powered by LearnLinc

Module: Digital Electronics
(in two parts)

- Text: "Digital Logic Tutorial ," Ken Bigelow, http://www.play-hookey.com/digital/
- References:
  - "Electronics Tutorial", part 10 (Thanks to Alex Pounds) http://doctord.dyndns.org:8000/courses/Topics/Electronics/Alex_Pounds/Index.htm
- Contents:
  - 7 – Digital Electronics 1
    - 5 on-line sessions plus one lab and a quiz
  - 8 – Digital Electronics 2
    - 5 on-line sessions plus one lab and a quiz
- Mastery Test part 4 follows this Module

Section 7: Digital Electronics 1

- Logic gates and Boolean algebra
- Truth Tables
- Binary numbers
- Memory
- Flip-Flops

Section 8: Digital Electronics 2

- Clocks and Counters
- Shift Registers
- Decoders
- Multiplexers & Demultiplexers
- Sampling

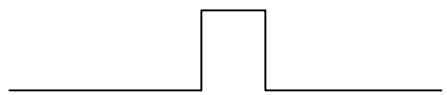
- **MT4**

Section 8 Schedule

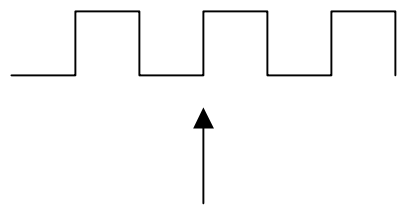
Session 8a	**04/02**	**Clocks and Counters**	**“Hookey”: “Counter” pages Alex Pounds: Part 27**
Session 8b	04/07	Shift Registers	“Hookey”: “Register” pages
Session 8c	04/09	Decoders	“Hookey”: Decoders and Demultiplexers
Session 8d	04/14	Multiplexers and Demultiplexers	“Hookey”: Multiplexers, Decoders and Demultiplexers
Session 8e	04/16	Sampling (A/D & D/A)	Notes
Session 8f (Quiz 8 due 04/27) (Lab - 04/26, Sat.)	04/21	Review for Quiz 7	
Session 8g	04/28	Quiz Results	
Session 8h	04/30	MT4 Q&A	
MT4	05/03		
MT4 Results	05/05		

Pulses and Clocks

- Single Pulse
  - Signal normally low then high for a short time and goes back to low



- Clock
  - Signal alternates high-low at a regular rate



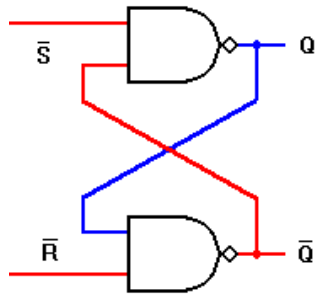
Positive going edge

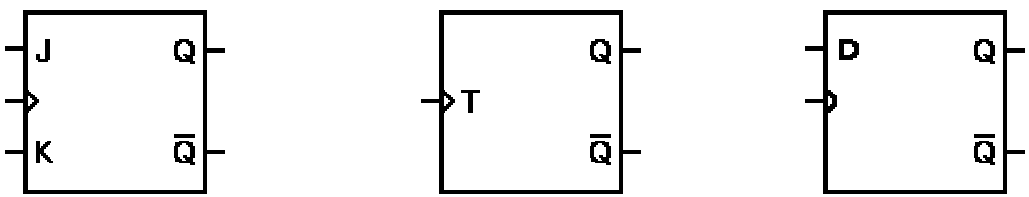
Clock

- Sets system speed
  - Data propagates at each clock cycle (edge)
  - Clock cannot be faster than a few gate delays
- Synchronizes system operation
  - Inputs from different parts of the circuit arrive "simultaneously" (within a few clock delays)
  - Reliable operation; few timing problems

Bit Storage

- The RS Latch (a "bit" of storage)
  - Set = 1: Q=1
  - Reset = 1: Q=0
- Register (n-bits of storage)
  - n latches (or flip-flops)
  - Stores a word (or byte) of data
- Flip-Flops
  - JK, T, D

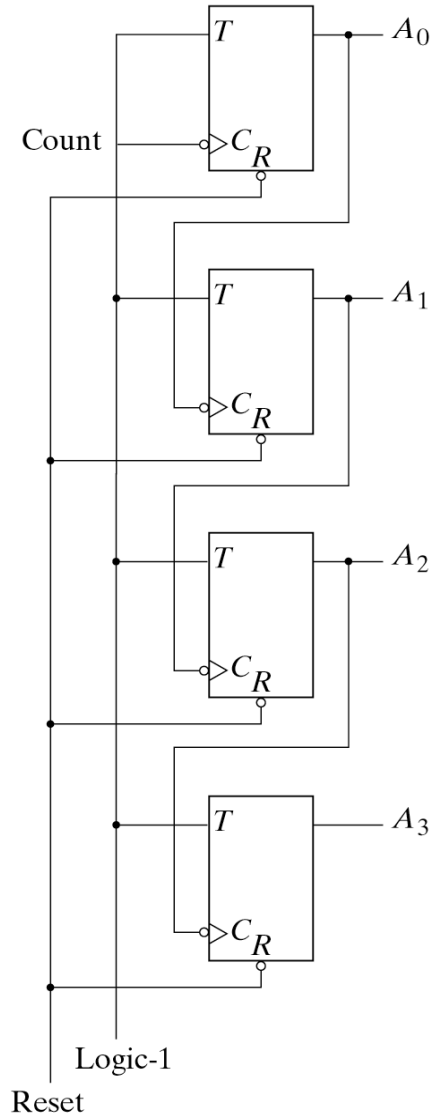




Binary Ripple Counter

- Asynchronous counter
- Changes “ripple” Through the stages on each clock edge

A_3	A_2	A_1	A_0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0



Synchronous Binary Counter

- All transitions occur on clock pulse edges in parallel
- Faster results than ripple counters

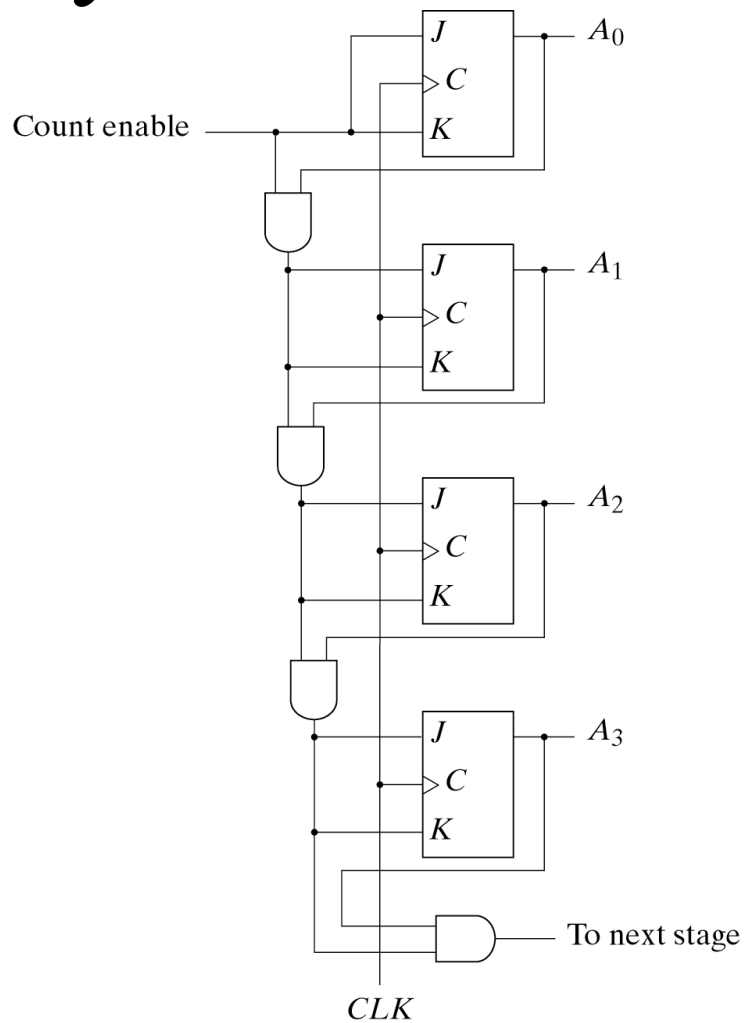
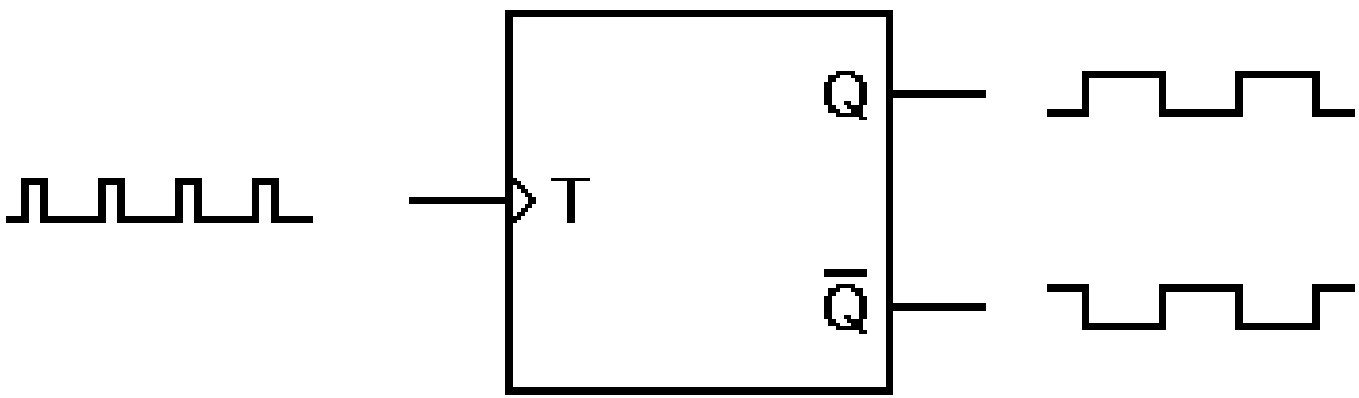


Fig. 6-12 4-Bit Synchronous Binary Counter

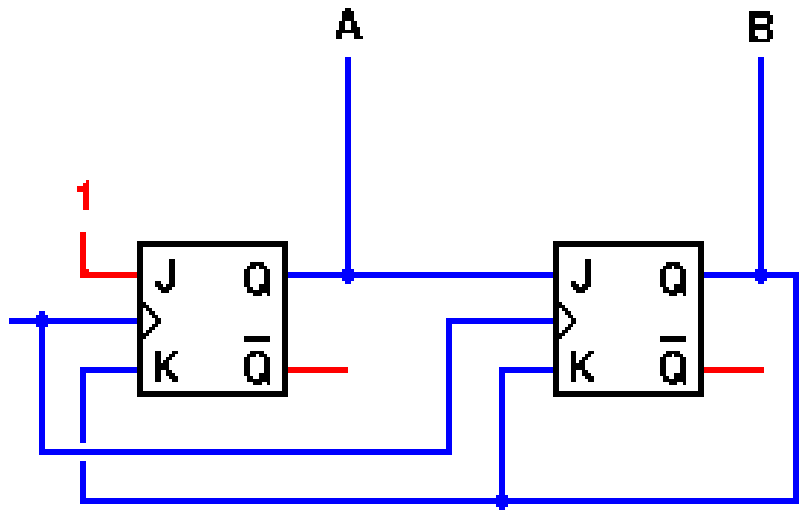
Binary Frequency Divider

- T Flip-Flop output
  - Frequency is ½ of the input clock rate
  - 50% duty cycle (even if the clock is not 50-50)
  - Q and Q′ are inverted versions of each other
- Divide by 2^n uses n binary dividers



Frequency Divide by 3

- You can divide the clock frequency by any number
- No longer a 50% duty cycle
- To divide by 6
  - First divide by 3
  - Then divide by 2 (now 50% again)



Simulation

- We'll again go to www.play-hookey.com/digital to see counters in action

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