Decoders

Part 8c of
"Electronics and Telecommunications"
A Fairfield University E-Course
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Module: Digital Electronics
(in two parts)

- Text: "Digital Logic Tutorial ," Ken Bigelow, http://www.play-hookey.com/digital/
- References:
  - "Electronics Tutorial", part 10 (Thanks to Alex Pounds) http://doctord.dyndns.org:8000/courses/Topics/Electronics/Alex_Pounds/Index.htm
- Contents:
  - 7 – Digital Electronics 1
    - 5 on-line sessions plus one lab and a quiz
  - 8 – Digital Electronics 2
    - 5 on-line sessions plus one lab and a quiz
- Mastery Test part 4 follows this Module

Section 7: Digital Electronics 1

- Logic gates and Boolean algebra
- Truth Tables
- Binary numbers
- Memory
- Flip-Flops

Section 8: Digital Electronics 2

- Clocks and Counters
- Shift Registers
- Decoders
- Multiplexers & Demultiplexers
- Sampling

- **MT4**

Section 8 Schedule

Session 8a	04/02	Clocks and Counters	"Hookey": "Counter" pages Alex Pounds: Part 27
Session 8b	04/09	Shift Registers	"Hookey": "Register" pages
Session 8c	**04/14**	**Decoders**	**"Hookey": Decoders and Demultiplexers**
Session 8d	04/16	Multiplexers and Demultiplexers	"Hookey": Multiplexers, Decoders and Demultiplexers
Session 8e	04/21	Sampling (A/D & D/A)	Notes
Session 8f (Quiz 8 due 04/27)	04/23	Review for Quiz 7	
Session 8g	04/28	Quiz Results	
Session 8h (Lab - 05/03, Sat.)	04/30	MT4 Q&A	
MT4 (sat, Meriden)	05/10		
MT4 Results	05/12		

Shift Register Review

- Cascade chain of Flip-Flops
- Data marches down the line at the beat of the clock
- Parallel or serial load, Parallel or serial read
- Applications:
  - Parallel to serial (serial transfer of data)
  - Serial to parallel (serial reception of data)
  - Feedback shift registers

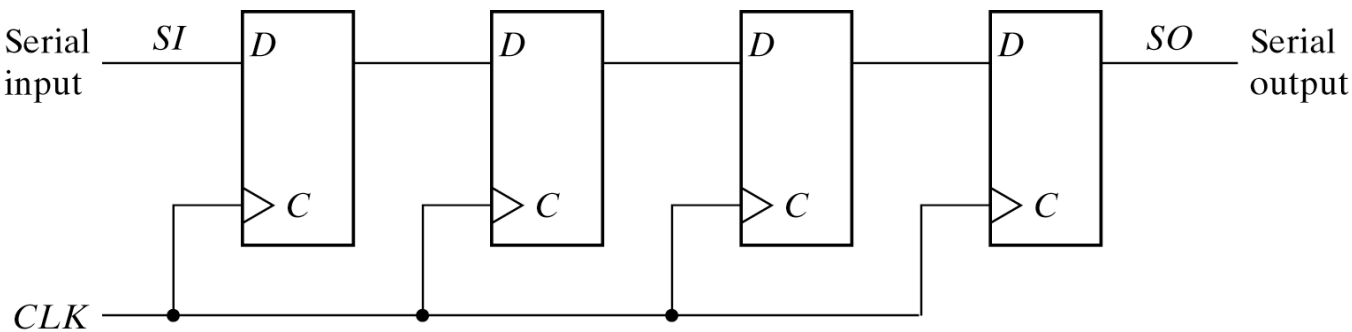
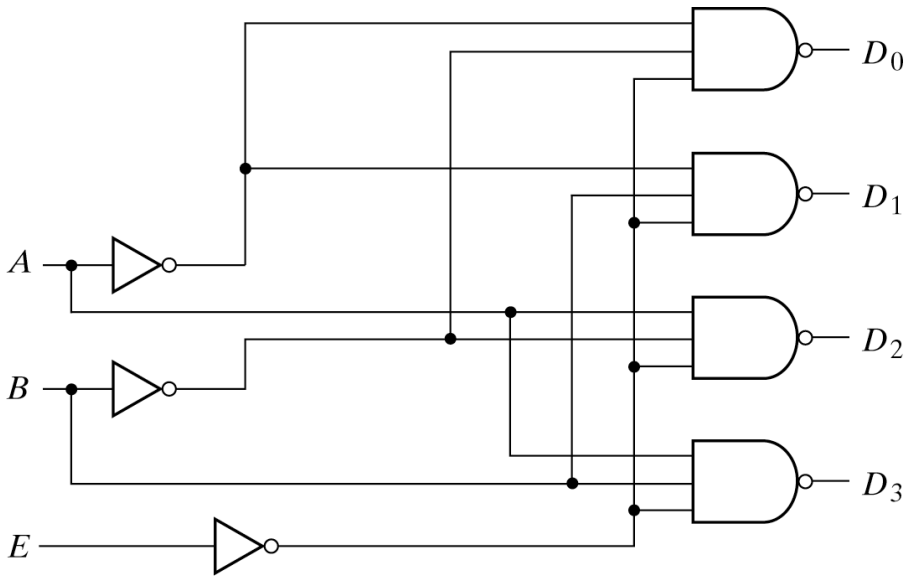


Fig. 6-3 4-Bit Shift Register

Decoders

- A small number of input bits; treated as a binary number
- A larger set of output bits (up to 2^n)
- The output bit values are “decoded” from the combination of the input bits
- Examples:
  - 1 of N decoding (Line Decoder)
  - Seven segment display decoder
  - BCD to Decimal line decoder

2-to-4 Line Decoder with Enable



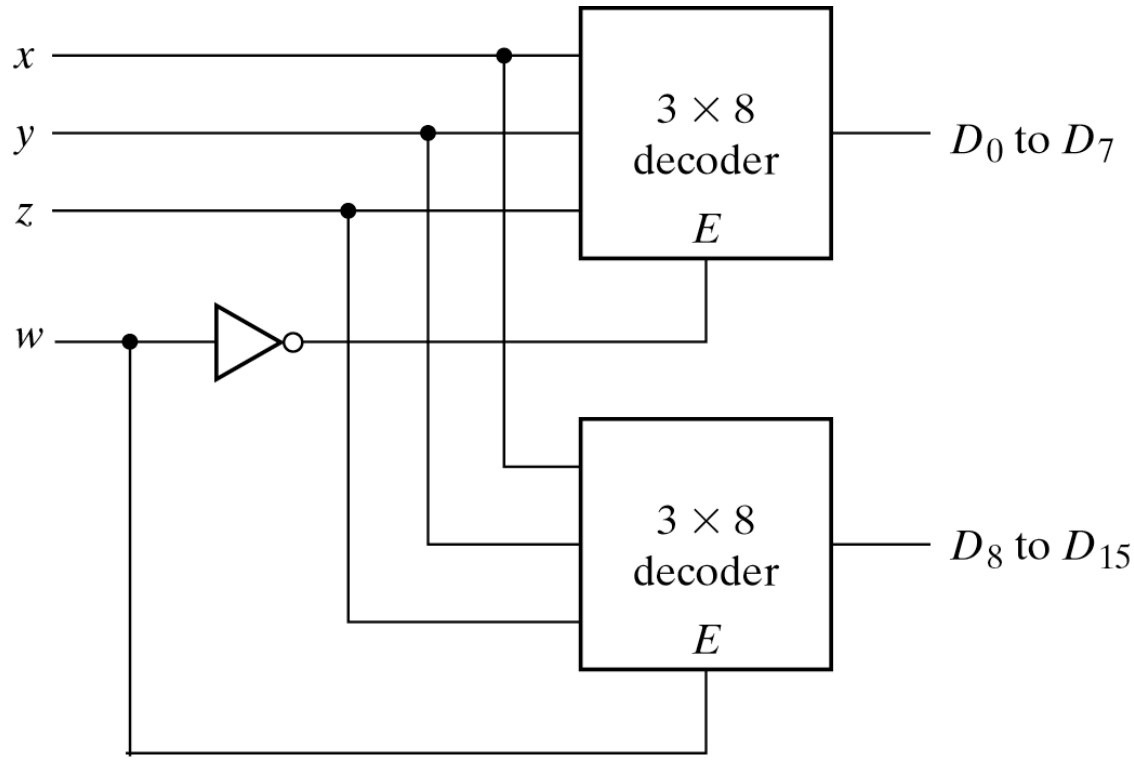
(a) Logic diagram

E	A	B	D_0	D_1	D_2	D_3
1	X	X	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0

(b) Truth table

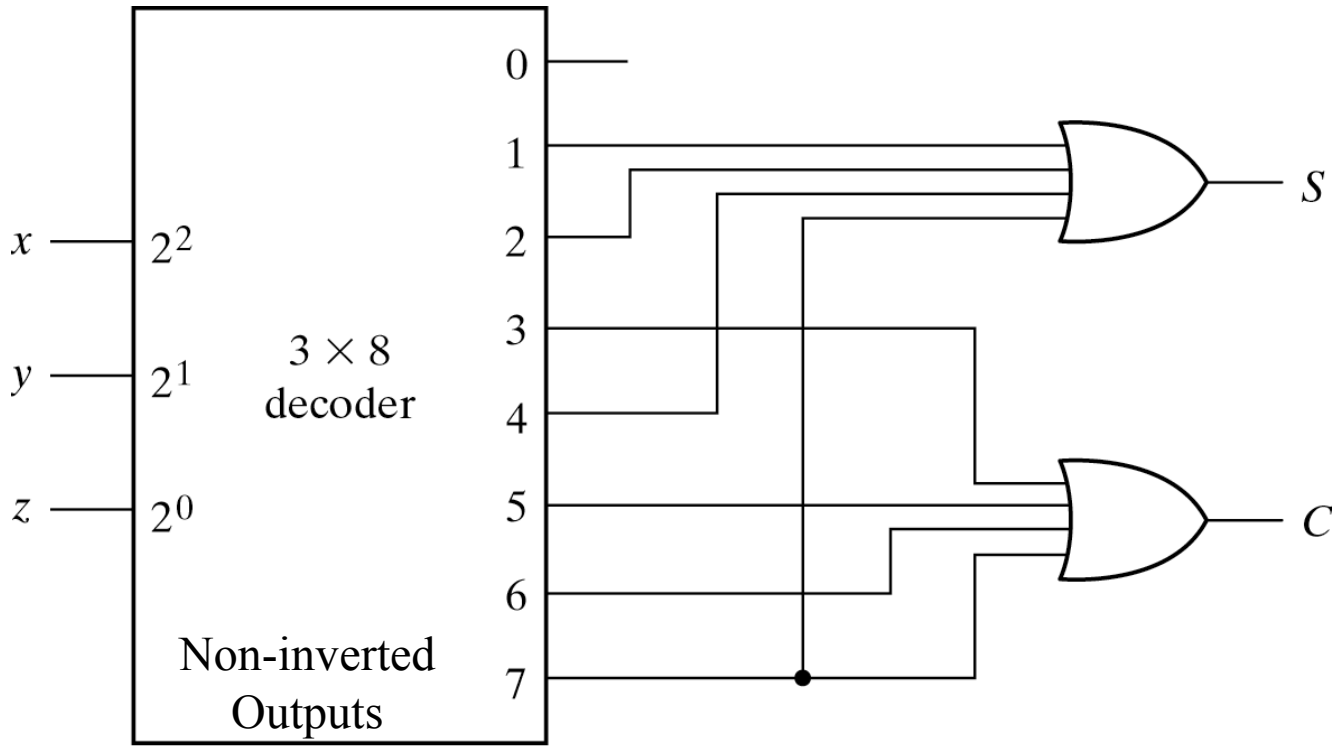
- The two input bits (A and B) select one of four outputs
  - Inverted outputs (active low)
  - Non-inverted outputs (active high)
- The Enable input must be low for decoder operation

Building Large Line Decoders



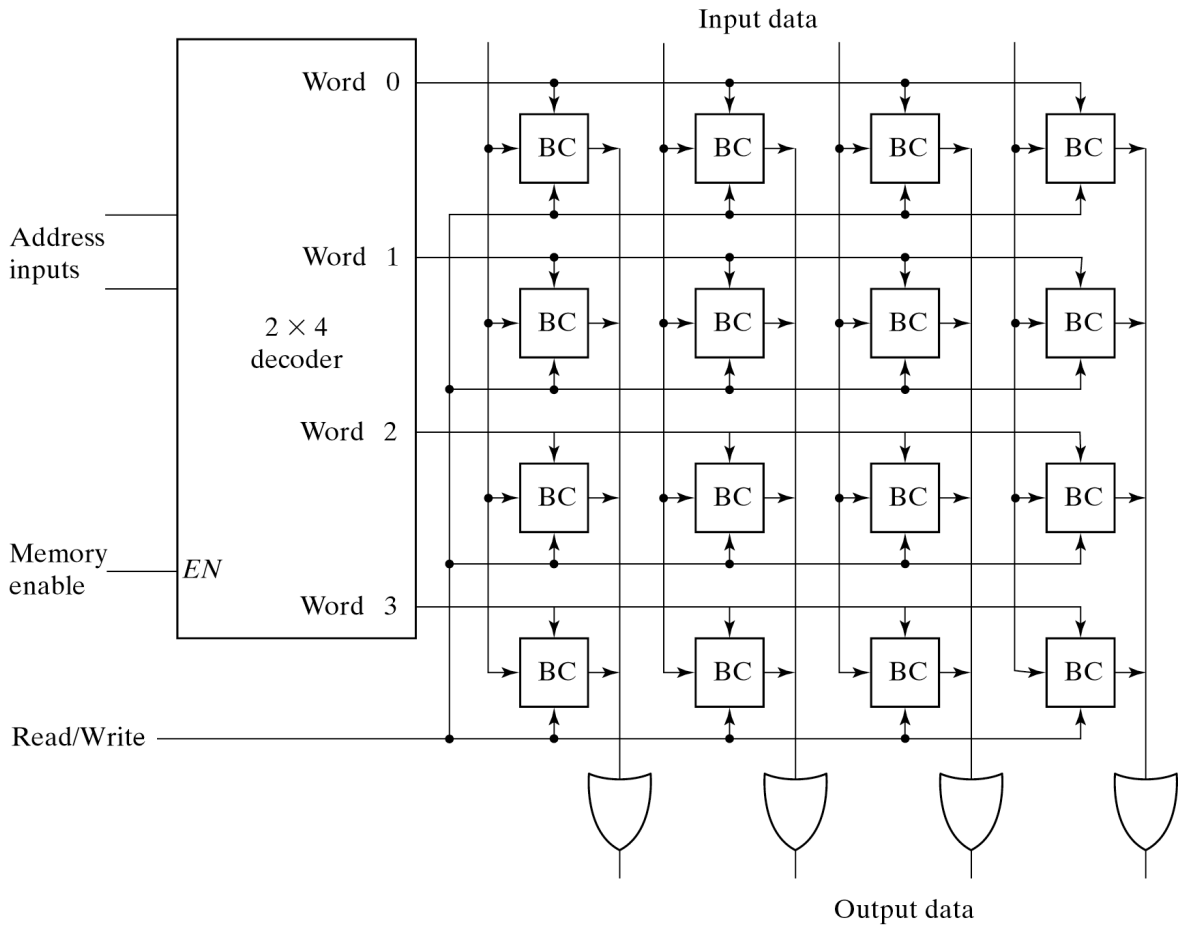
- The Enable control allows the construction of large decoders from a set of small decoders

Full Adder Via a Line Decoder



- Line decoders can be used to implement complex logical functions

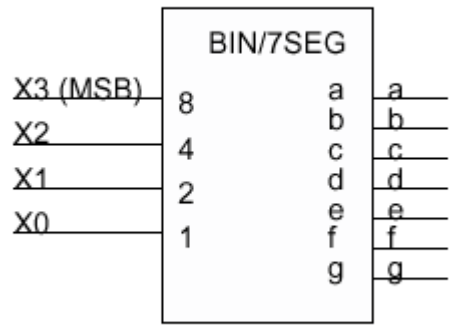
A 4 x 4 RAM

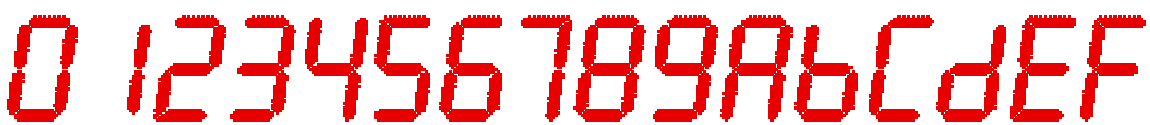


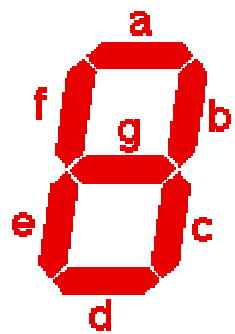
- Address decoder provides “word select”

7-Segment Decoder

- Four input bits
- Seven segment LED's enabled to show desired character
- Some displays also have a decimal point







Simulation

- We'll again go to www.play-hookey.com/digital to see Decoders in action

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