Review for Quiz 8

Part 8f of
"Electronics and Telecommunications"
A Fairfield University E-Course
Powered by LearnLinc

Module: Digital Electronics
(in two parts)

- Text: "Digital Logic Tutorial ," Ken Bigelow, http://www.play-hookey.com/digital/
- References:
  - "Electronics Tutorial", part 10 (Thanks to Alex Pounds) http://doctord.dyndns.org:8000/courses/Topics/Electronics/Alex_Pounds/Index.htm
- Contents:
  - 7 – Digital Electronics 1
    - 5 on-line sessions plus one lab and a quiz
  - 8 – Digital Electronics 2
    - 5 on-line sessions plus one lab and a quiz
- Mastery Test part 4 follows this Module

Section 7: Digital Electronics 1

- Logic gates and Boolean algebra
- Truth Tables
- Binary numbers
- Memory
- Flip-Flops

Section 8: Digital Electronics 2

- Clocks and Counters
- Shift Registers
- Decoders
- Multiplexers & Demultiplexers
- Sampling

- **MT4**

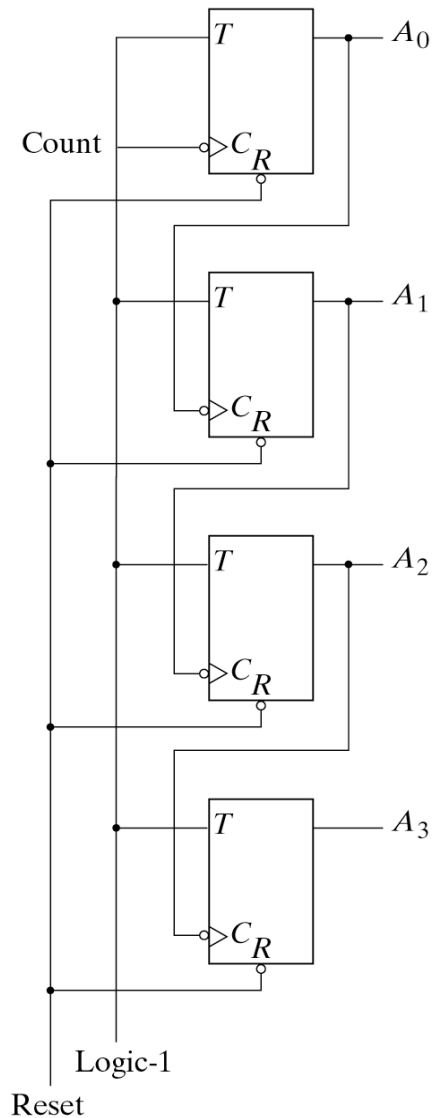
Section 8 Schedule

Session 8a	04/02	Clocks and Counters	"Hookey": "Counter" pages Alex Pounds: Part 27
Session 8b	04/09	Shift Registers	"Hookey": "Register" pages
Session 8c	04/14	Decoders	"Hookey": Decoders and Demultiplexers
Session 8d	04/16	Multiplexers and Demultiplexers	"Hookey": Multiplexers, Decoders and Demultiplexers
Session 8e	04/21	Sampling (A/D & D/A)	Notes
Session 8f (Quiz 8 due 04/27)	**04/23**	**Review for Quiz 8**	
Session 8g	04/28	Quiz Results	
Session 8h (Lab - 05/03, Sat.)	04/30	MT4 Q&A	
MT4 (Sat, Cheshire)	05/10		
MT4 Results	05/12		

Counter Review

- Clock: Sets system speed
- Bit Storage: Latch or Flip-Flop
- Register (n-bits of storage)
- Counters
  - Ripple Counter
  - Synchronous Counter
- Frequency Divider:

  Counter Divides clock rate by an integer



Shift Register Review

- Cascade chain of Flip-Flops
- Data marches down the line at the beat of the clock
- Parallel or serial load, Parallel or serial read
- Applications:
  - Parallel to serial (serial transfer of data)
  - Serial to parallel (serial reception of data)
  - Feedback shift registers

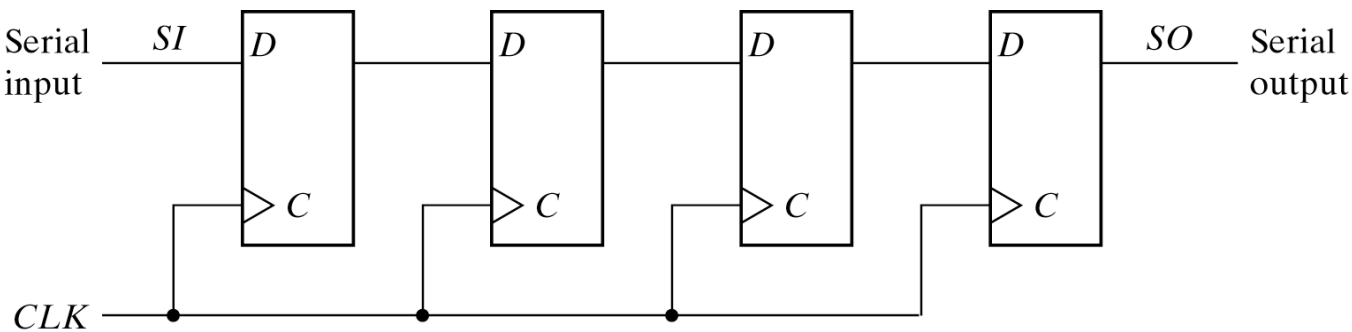
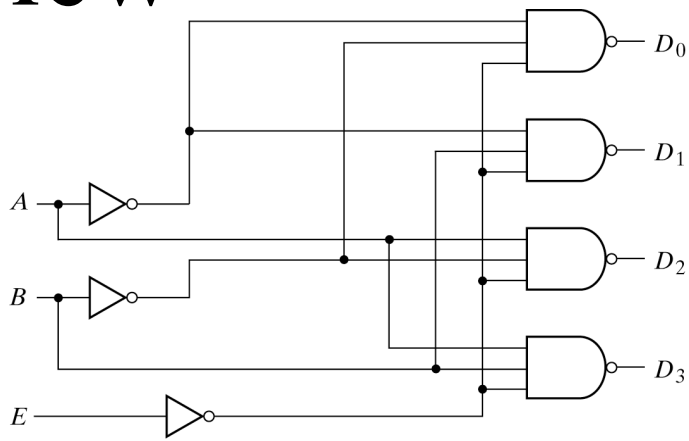
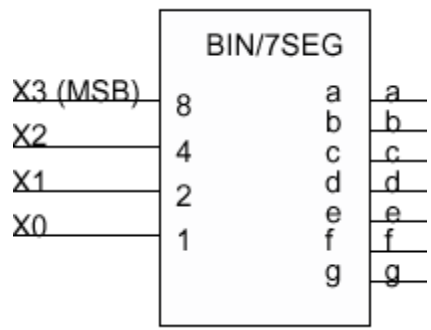


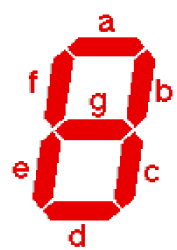
Fig. 6-3 4-Bit Shift Register

Decoder Review

- A small number of input bits; treated as a binary number
- A larger set of output bits (up to 2^n)
- The output bit values are "decoded" from the combination of the input bits
- Examples:
  - 1 of N decoding
    - Line Decoder
    - Address Decoder
  - Seven segment display decoder
  - BCD to Decimal line decoder



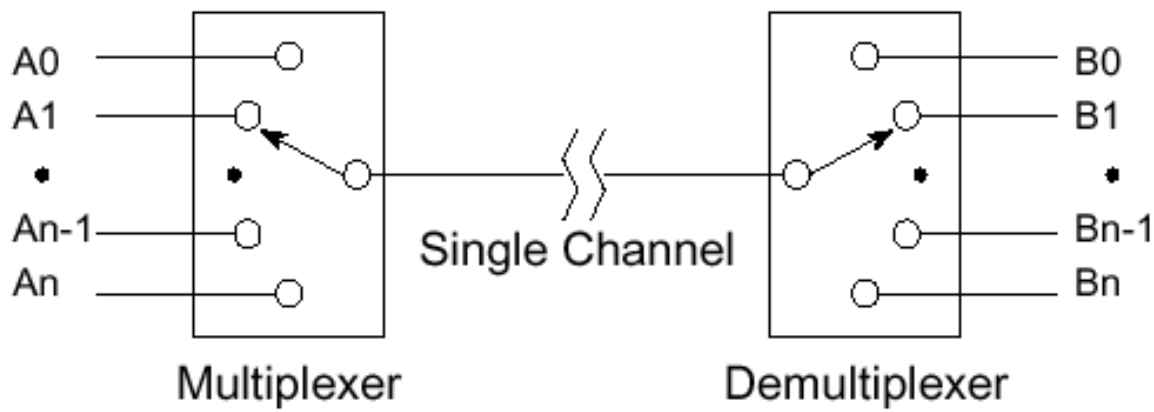




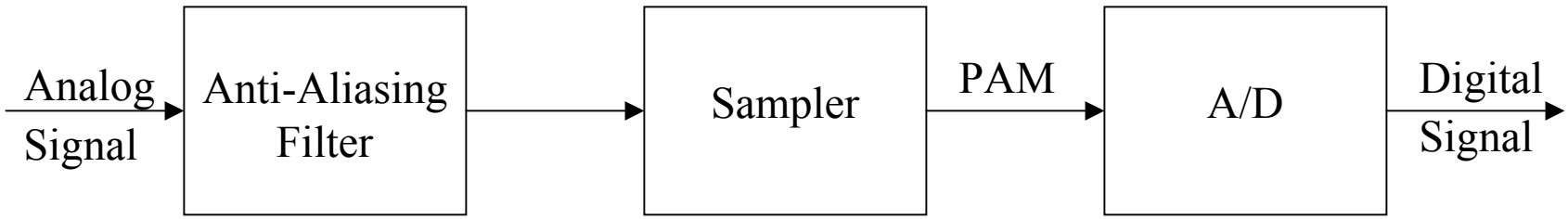
Mux and Demux Review

4.4 Multiplexer

- Multilexer - A ***data selector*** that selects one of may inputs to appear on a single output line
- Demultiplexer - A ***data distributor*** that takes a single input line and routes it to one of several output lines

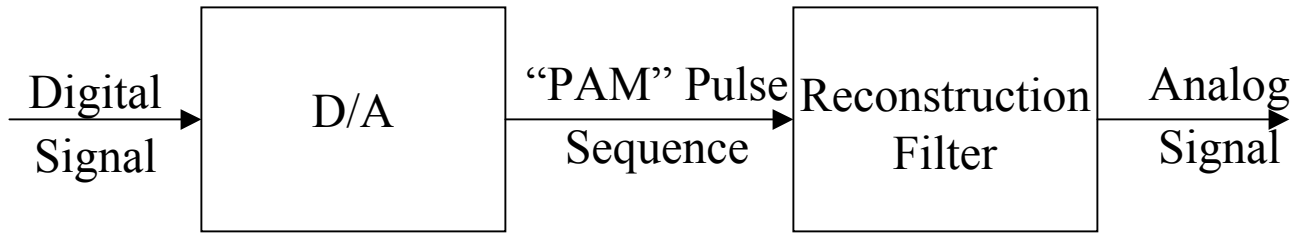


Analog to Digital Conversion



- **Analog Signal:** A continuous electrical signal
- **Aliasing:** Confusion of high and low frequencies if sampling is too slow (filter ensures Nyquist criterion; Nyquist rate $f_s > 2\ f_{max}$ to avoid aliasing)
- **Sampling:** The process of approximating an analog signal by a sequence of narrow pulses
- **A/D:** Representing the "strength" of a pulse by a binary number (introduces an error due to word length)

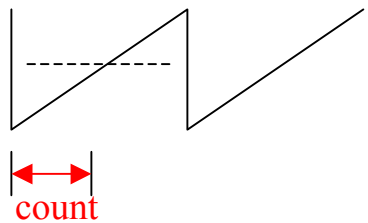
Digital to Analog Conversion



- **Digital Signal:** A sequence of binary numbers representing an analog signal (approximate – digital "noise")
- **PAM:** Pulse Amplitude Modulation - A sequence of pulses with strengths corresponding to the analog signal
- **Reconstruction Filter:** Averaging out the pulse sequence to reproduce the original analog signal (almost identical to the "anti-aliasing filter")

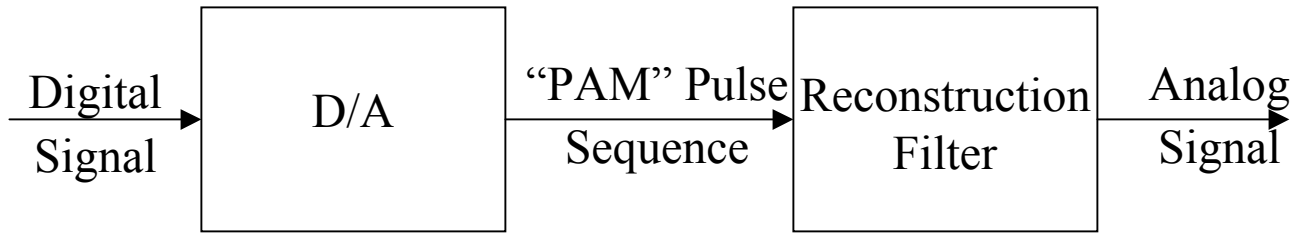
Analog to Digital Conversion

- Flash (or parallel)A/D
  - Very fast
  - Either low resolution (8-bits) or very expensive
- Successive approximation A/D
  - Determines the MSB first
  - Repeatedly refines the representation
  - Accurate (high resolution) but slow
- Counting A/D: Uses a ramp signal and a high speed counter to determine the time that the ramp exceeds the signal value



- Over-Sampled (Sigma-Delta) A/D
  - Flash encodes a low-resolution value at high speeds
  - Uses a digital filter (anti-alias) to lower the bandwidth
    - Allows reduction of the sampling rate
    - Improves the resolution (number of bits)

Digital to Analog Conversion



- Reverses the A/D sequence
- D/A: generates a PAM pulse sequence where each pulse magnitude corresponds to the value of the corresponding digital number
- Reconstruction filter: Almost identical to the Anti-Aliasing filter used in A/D. Smoothes out the pulse sequence to reproduce the original signal.

Applications

- North American Telephony (64 kbits/sec)
  - Sampling rate = 8 kHz (3 dB: 3.3 kHz , f_{max}: 3.8 kHz)
  - μ255 (logarithmic), 8-bit words (256 levels)
- CD Audio
  - Sampling rate = 44.1 kHz per channel (3 dB: 20 kHz, f_{max}: 21 kHz) (note: DAT = 48 kHz - Prof Audio = 96 kHz, 24 bit)
  - Linear 16-bit words
- PC sound card:
  - Sampling rate = 8, 16, 11.025, 22.05, 44.1 kHz
  - 8 or 16 bit word size

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