Digital Design
Lecture 14

ROMs and RAMs
Mano, 7.6-7.8

PLD Configurations

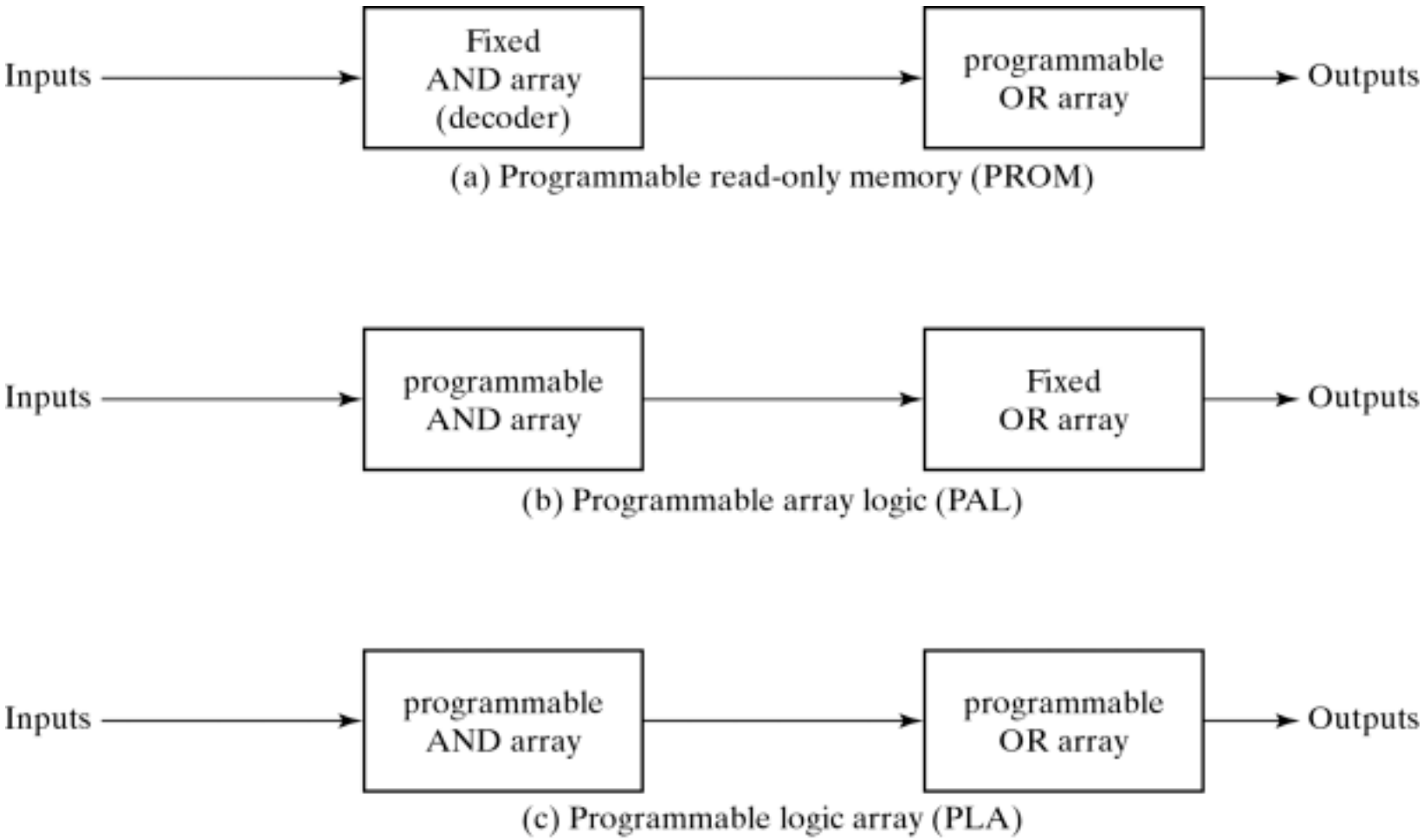


Fig. 7-13 Basic Configuration of Three PLDs

An Example PLA

- Buffers provide true and complement of inputs
- XORs provide programmable complementors on outputs
- Similar to PROM
  - Partial variable decoding
  - Only some minterms

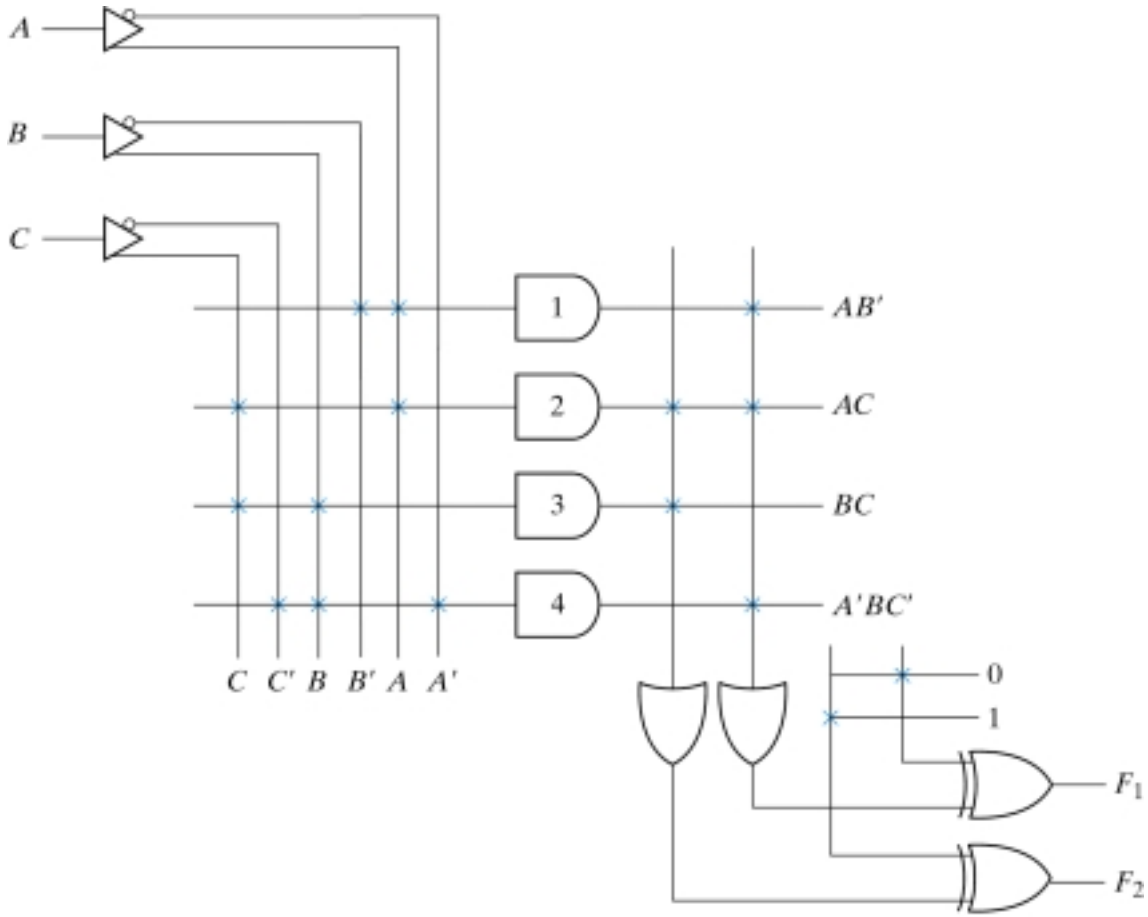


Fig. 7-14 PLA with 3 Inputs, 4 Product Terms, and 2 Outputs

PLA Programming Table

		Inputs			Outputs	
Product Term		**A**	**B**	**C**	**(T) F_1**	**(C) F_2**
AB′	1	1	0	-	1	-
AC	2	1	-	1	1	1
BC	3	-	1	1	-	1
A′BC′	4	0	1	0	1	-

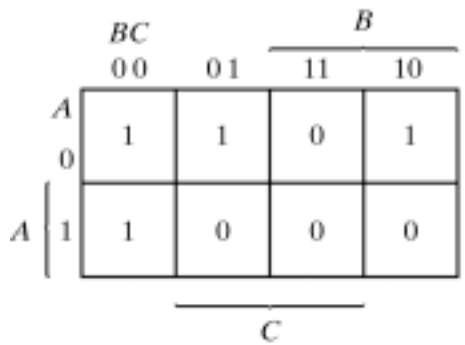
Table 7-5

Solution to Example 7-2

Implement

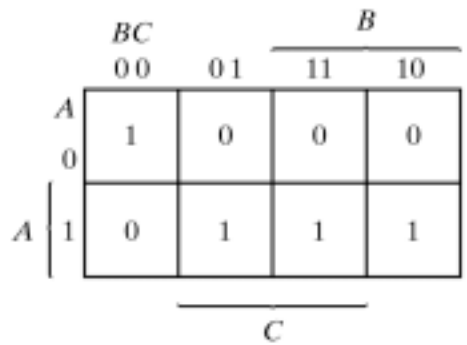
$F_1(A,B,C)=\Sigma(0,1,2,4)$

$F_2(A,B,C)=\Sigma(0,5,6,7)$



$F_1 = A'B' + A'C' + B'C'$

$F_1 = (AB + AC + BC)'$



$F_2 = AB + AC + A'B'C'$

$F_2 = (A'C + A'B + AB'C')'$

PLA programming table

	Product term	Inputs A	B	C	Outputs (C) F_1	(T) F_2
AB	1	1	1	–	1	1
AC	2	1	–	1	1	1
BC	3	–	1	1	1	–
$A'B'C'$	4	0	0	0	–	1

Fig. 7-15 Solution to Example 7-2

Programmable Array Logic

- Fixed OR array
- Programmable AND array

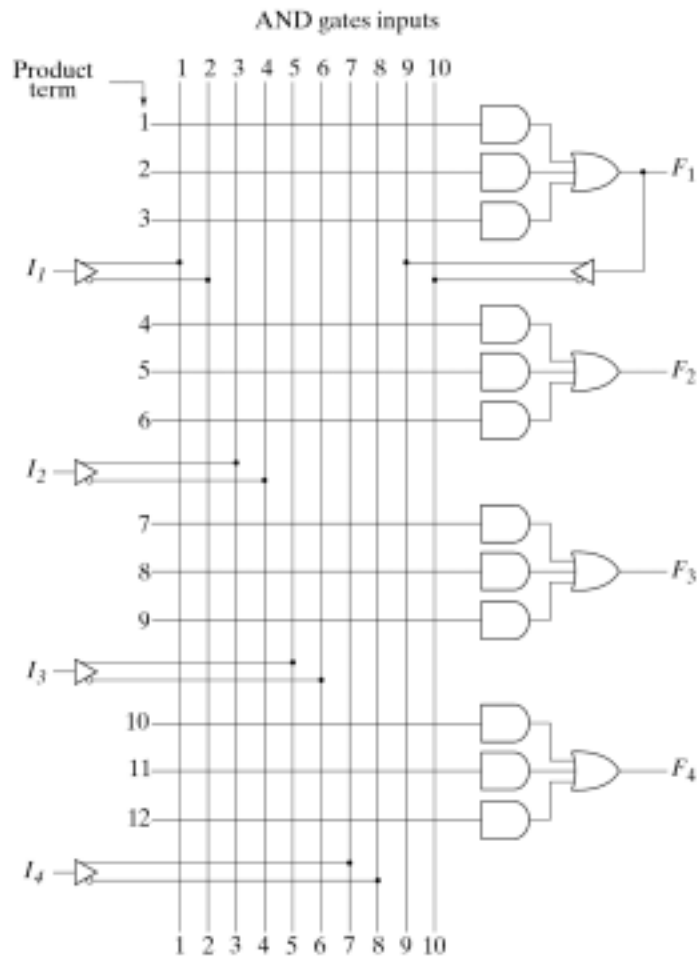


Fig. 7-16 PAL with Four Inputs, Four Outputs, and Three-Wide AND-OR Structure

PAL Fuse Map

PAL Programming Table

Product Term	AND Inputs					Outputs
	A	B	C	D	E	
1	1	1	0	-	-	$w = A B C' + A'B'C D'$
2	0	0	1	0	-	
3	-	-	-	-	-	$x = A + B C D$
4	1	-	-	-	-	
5	-	1	1	1	-	$y = A'B + C D + B'D$
6	-	-	-	-	-	
7	0	1	-	-	-	$z = w + A'C'D' + A'B'C'D$
8	-	-	1	1	-	
9	-	0	-	0	-	
10		-	-	-	1	
11	1	-	0	0	-	
12	0	0	0	1	-	

Table 7-6

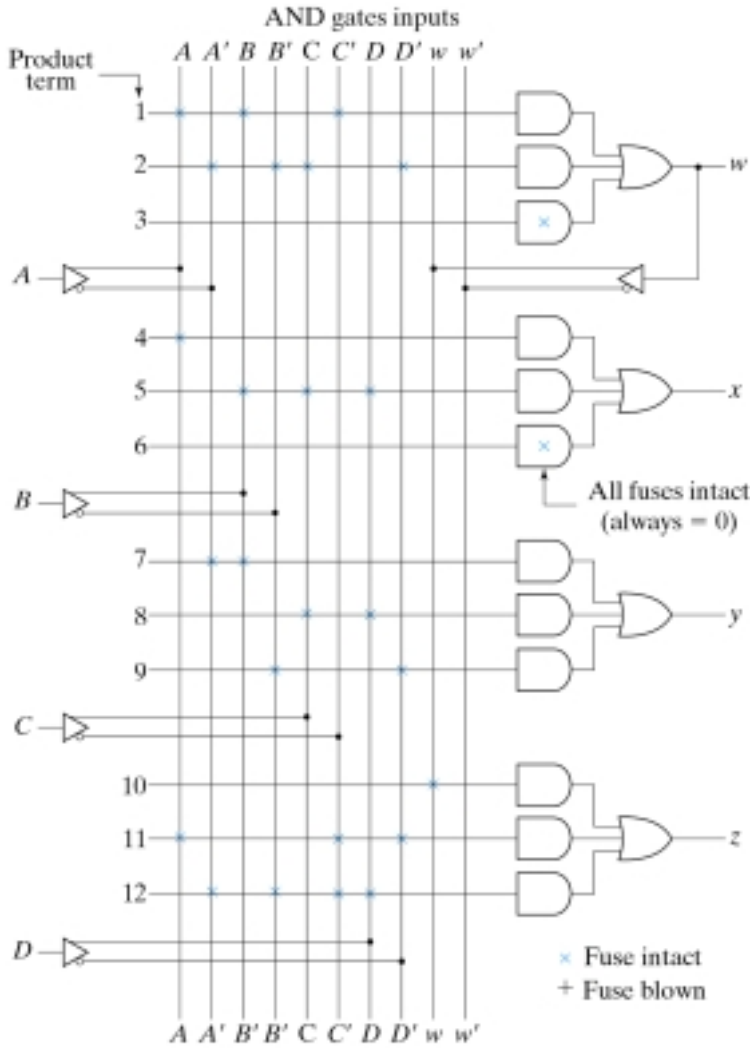


Fig. 7-17 Fuse Map for PAL as Specified in Table 7-6

Sequential PLDs

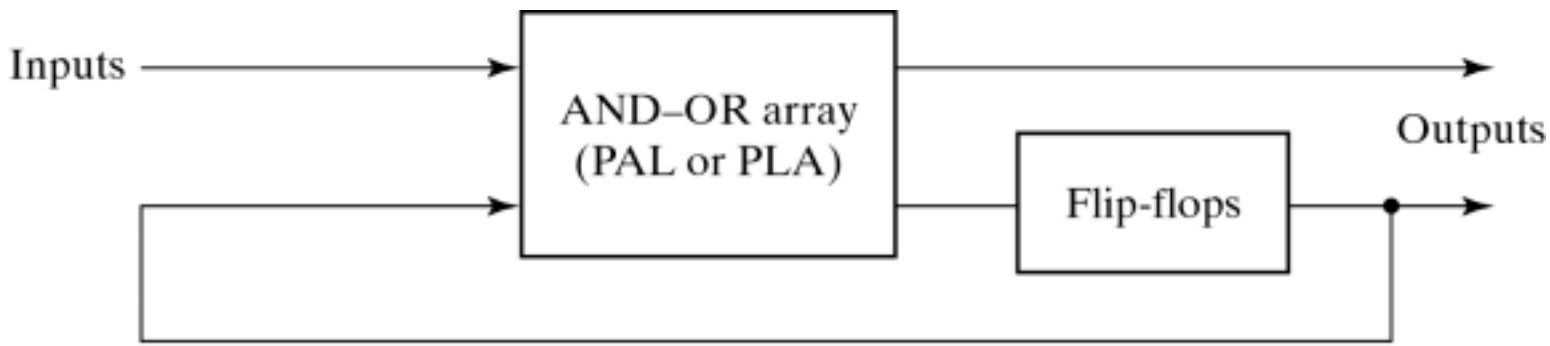


Fig. 7-18 Sequential Programmable Logic Device

Sequential Programmable Devices

- Sequential (simple) programmable Logic device (SPLD)
  - Field-programmable logic sequence (FPLS, defunct – too hard to use)
  - Registered PAL / macrocell structure
- Complex programmable logic device (CPLD)
  - Collection of SPLDs on a chip
- Field programmable gate array (FPLA)
  - Logic blocks (look-up tables, multiplexers, gates, flip-flops)
  - Programmable input/output blocks
  - Programmable interconnections
- Microprocessor (using PROM)

Macrocell Logic

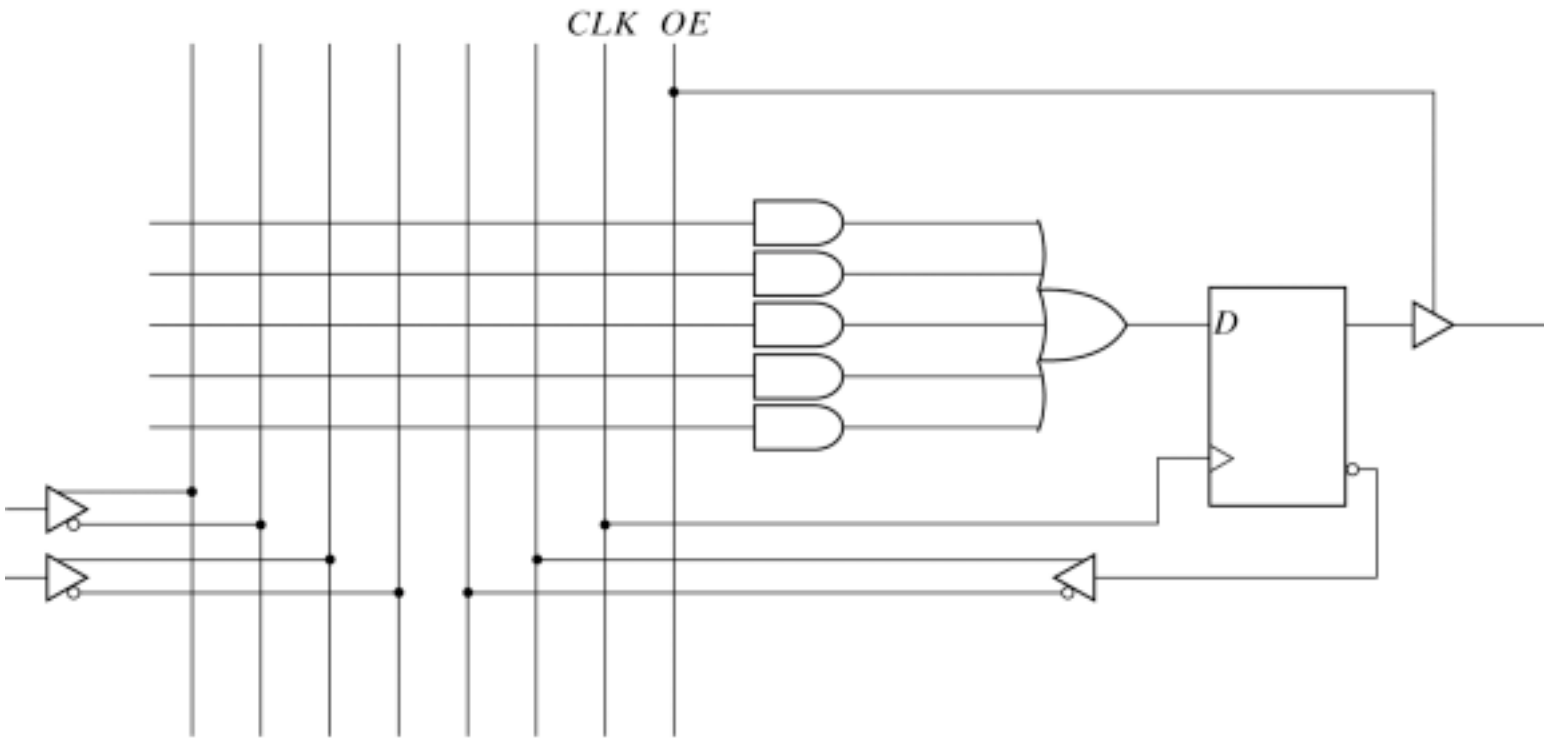


Fig. 7-19 Basic Macrocell Logic

CPLD

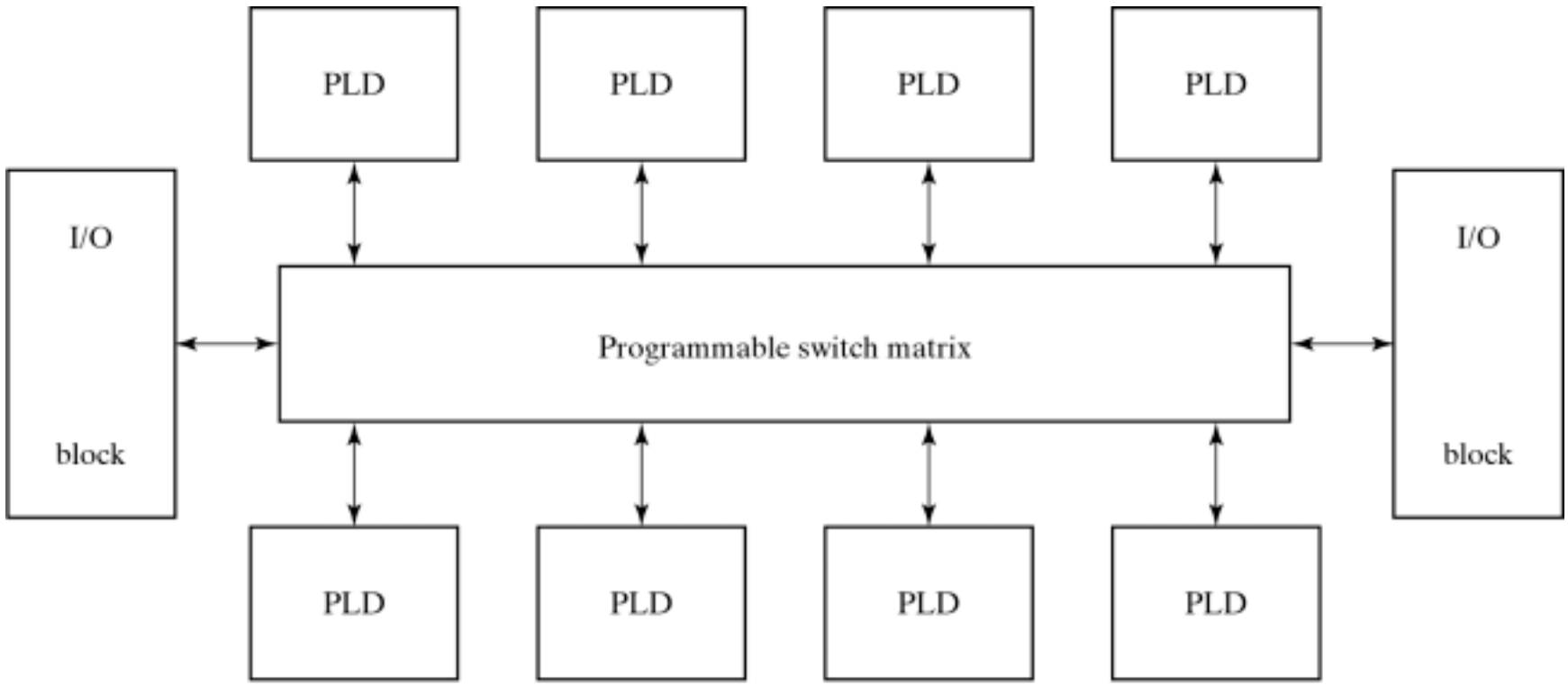


Fig. 7-20 General CPLD Configuration