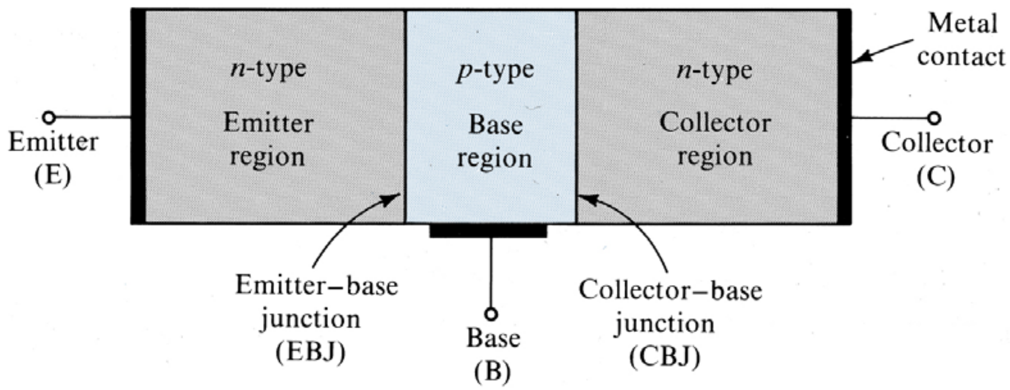
Week 4: Bipolar Junction Transistor

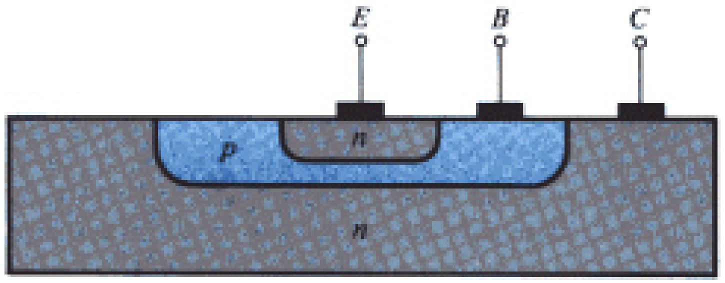
Topics to cover …

- Physical Operation and I-V Characteristics
- BJT Circuit Models
- DC Analysis
- BJT Biasing
- Reading Assignment:
  Chap 5.1-5.3, 5.5-5.9, 5.11, 10.1-10.3 of Jaeger & Blalock, or
  Chap 5.1-5.5 of Sedra & Smith

Bipolar Junction Transistor (BJT)

- *npn* transistor:





Vertical *npn*

- 3 terminals:
  - emitter, base, and collector
- 2 *pn* junctions:
  - emitter-base junction (EBJ)
  - collector-base junction (CBJ)
- Emitter: heavily doped
- Base: very thin

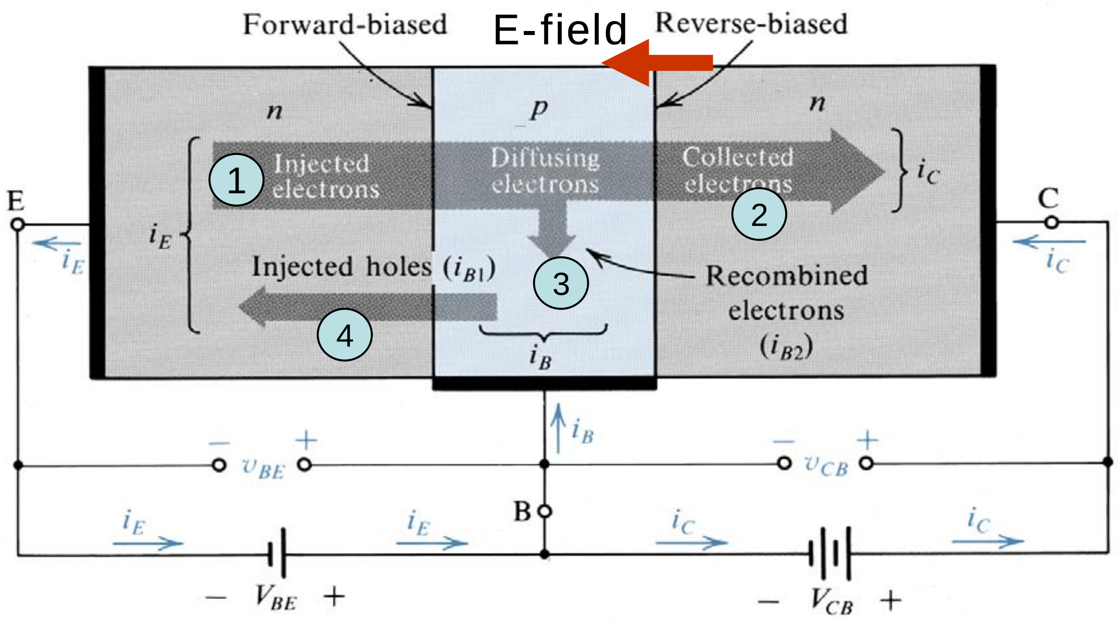
Regions of Operation

- Depends on the biasing across each of the junctions, different regions of operation are obtained:

Base-Emitter Junction	Base-Collector Junction	
	Reverse Bias	**Forward Bias**
Forward Bias	**Forward-active region** **(Active region)** (Good amplifier)	**Saturation region** (Closed switch)
Reverse Bias	**Cutoff region** (open switch)	**Reverse-active region** (Poor amplifier, rarely used)

BJT in Active Region

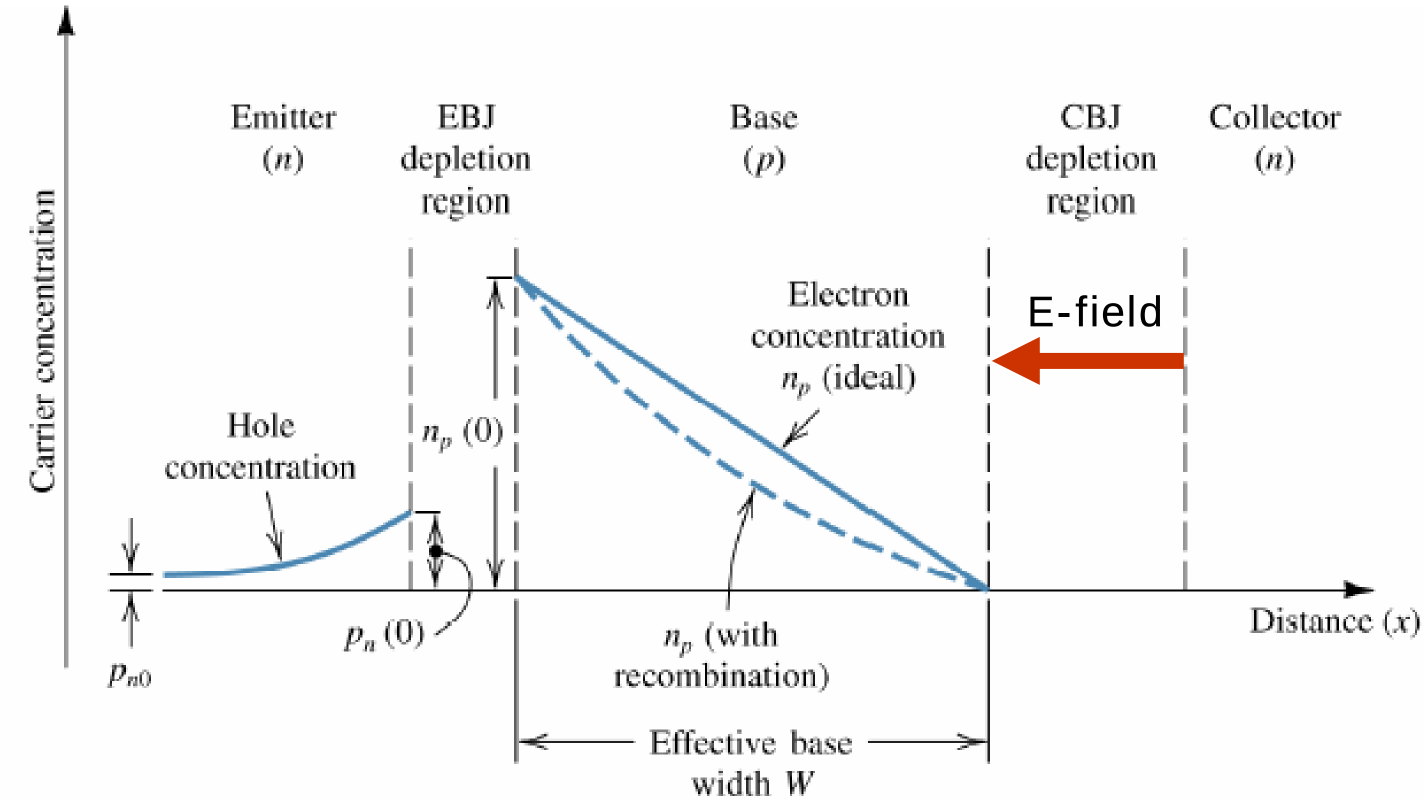
Biasing:
E-B: Forward
C-B: Reverse



Operation:

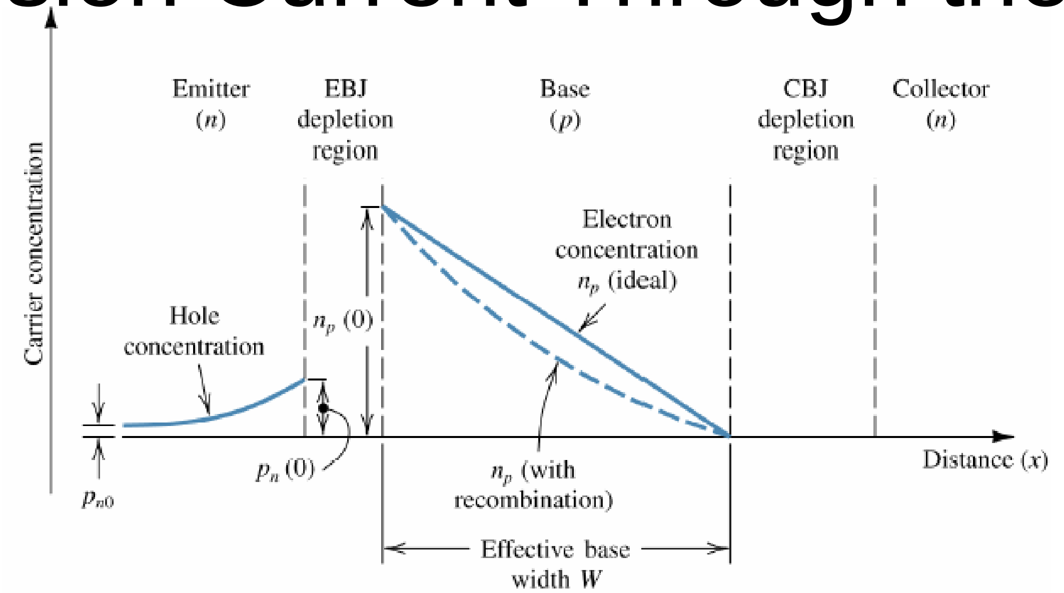
1. Forward bias of EBJ causes electrons to diffuse from emitter into base.
2. As base region is very thin, the majority of these electrons diffuse to the edge of the depletion region of CBJ, and then are swept to the collector by the electric field of the reverse-biased CBJ.
3. A small fraction of these electrons recombine with the holes in base region.
4. Holes are injected from base to emitter region. (4) << (1).

Minority Concentration Profiles



- Current dominated by electrons from emitter to base (by design) b/c of the forward bias and minority carrier concentration gradient through the base
  - some recombination causes bowing of electron concentration (in the base)

Diffusion Current Through the Base



i_C

- Diffusion of electrons through the base is set by concentration profile at the EBJ

$$n_p(0) = n_{p0} e^{v_{BE}/V_T}$$

- Diffusion current of electrons through the base is (assuming an ideal straight line case):

$$I_n = A_E q D_n \frac{dn_p(x)}{dx} = A_E q D_n \left(-\frac{n_p(0)}{W}\right)$$

- The collector current: $i_C = -I_n$ (- sign: current into collector)

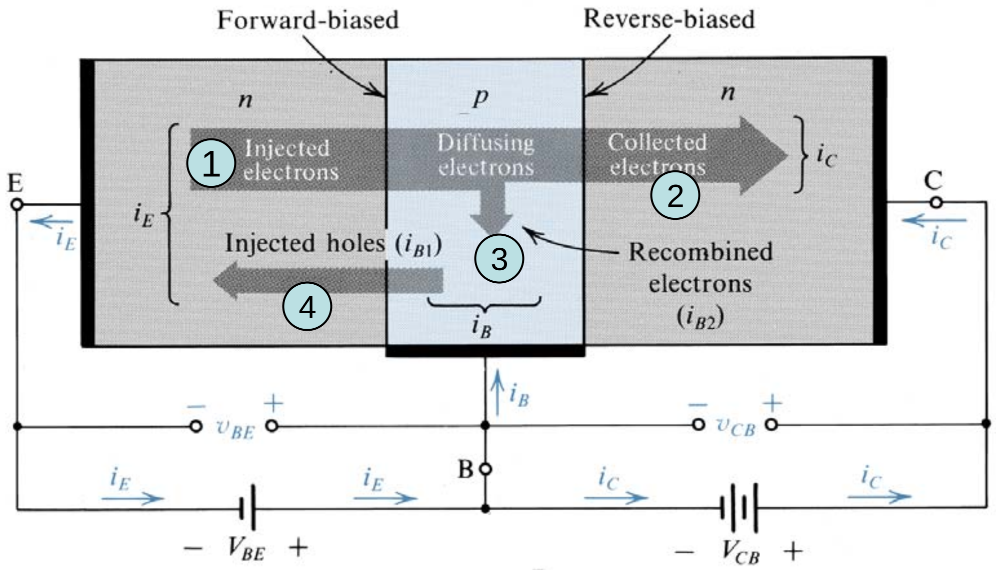
Collector Current

- The collector current:

$$\boxed{i_C = I_S e^{v_{BE}/V_T}} \qquad \text{where} \qquad I_S = \frac{qA_E D_n n_{p0}}{W} = \frac{qA_E D_n n_i^2}{N_A W}$$

- Note that i_C is independent of collector voltage.
- The current at the collector is controlled by the voltage across the other two terminals – a voltage controlled current source. This control is the basic transistor action.
- Saturation current I_S is
  – inversely proportional to W and directly proportional to A_E
    - Want short base and large emitter area for high currents
  – dependent on temperature due to n_i^2 term

Base Current



Base current consists of two components: i_{B1} and i_{B2}:

- i_{B1} , due to forward bias of EBJ, is an exponential function of v_{BE}.
- i_{B2} , due to recombination, is directly proportional to the numbers of electrons injected from the emitter, which in turn is an exponential function of v_{BE}.

$$\Rightarrow \quad i_B \propto e^{v_{BE}/V_T}$$

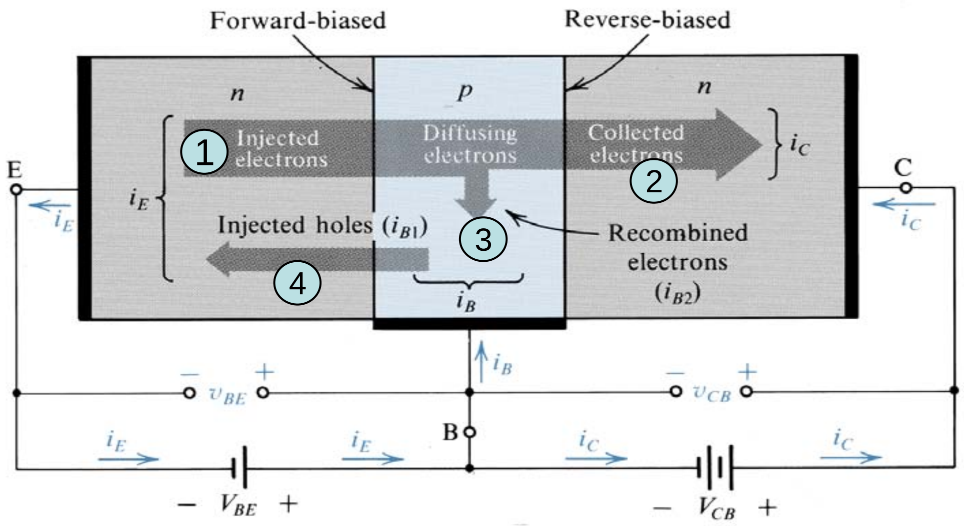
The Beta (β)

- Can relate i_B and i_C by the following equation

$$i_B = \frac{i_C}{\beta} = \frac{I_S}{\beta} e^{v_{BE}/V_T}$$

- $\beta = i_C / i_B$
  - β is constant for a particular transistor
  - On the order of 100-200 in modern devices (but can be higher)
  - called ***common-emitter current gain***.
  - also denoted as β_F.

Emitter Current



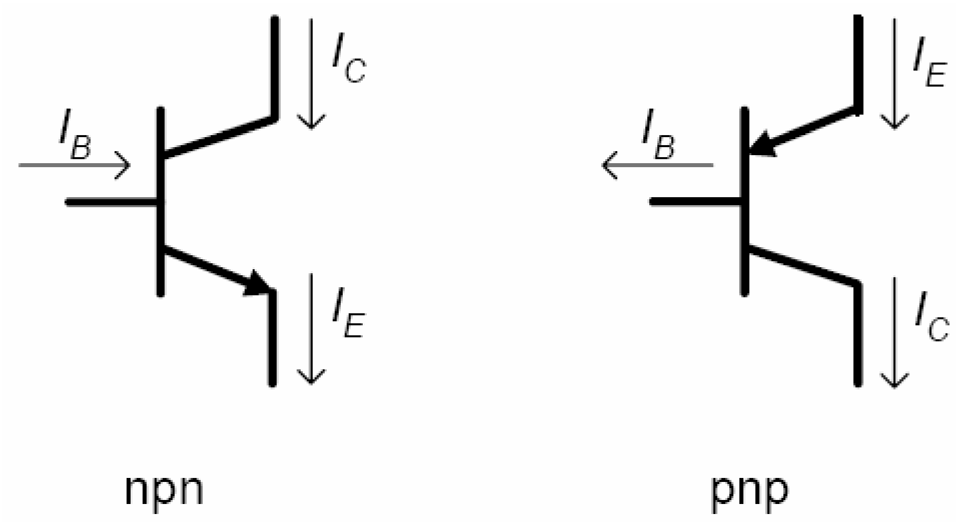
Treat transistor as a super-node, by KCL we obtain

$$i_E = i_B + i_C = \frac{1}{\beta} i_C + i_C = \frac{1+\beta}{\beta} i_C \qquad \text{or} \quad i_C = \frac{\beta}{1+\beta} i_E$$

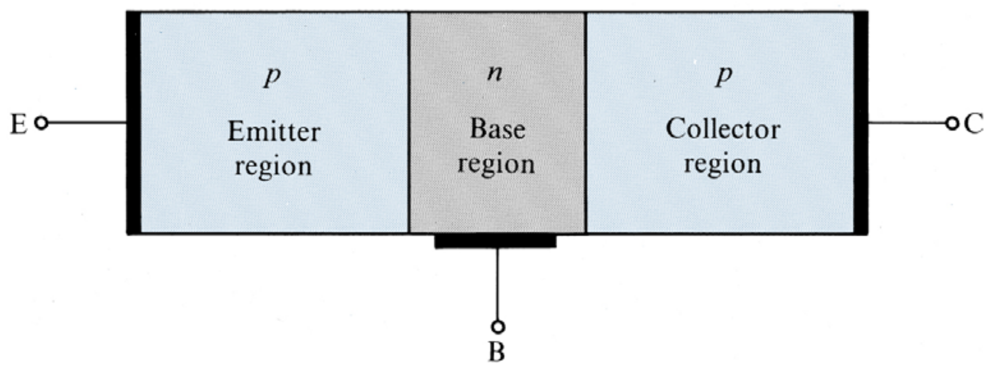
$$\therefore \quad \boxed{i_C = \alpha\, i_E} \quad \text{where} \quad \boxed{\alpha = \frac{\beta}{1+\beta}} \quad \text{or} \quad \boxed{\beta = \frac{\alpha}{1-\alpha}}$$

α is called ***common-base current gain***. α < 1 but very close to 1.

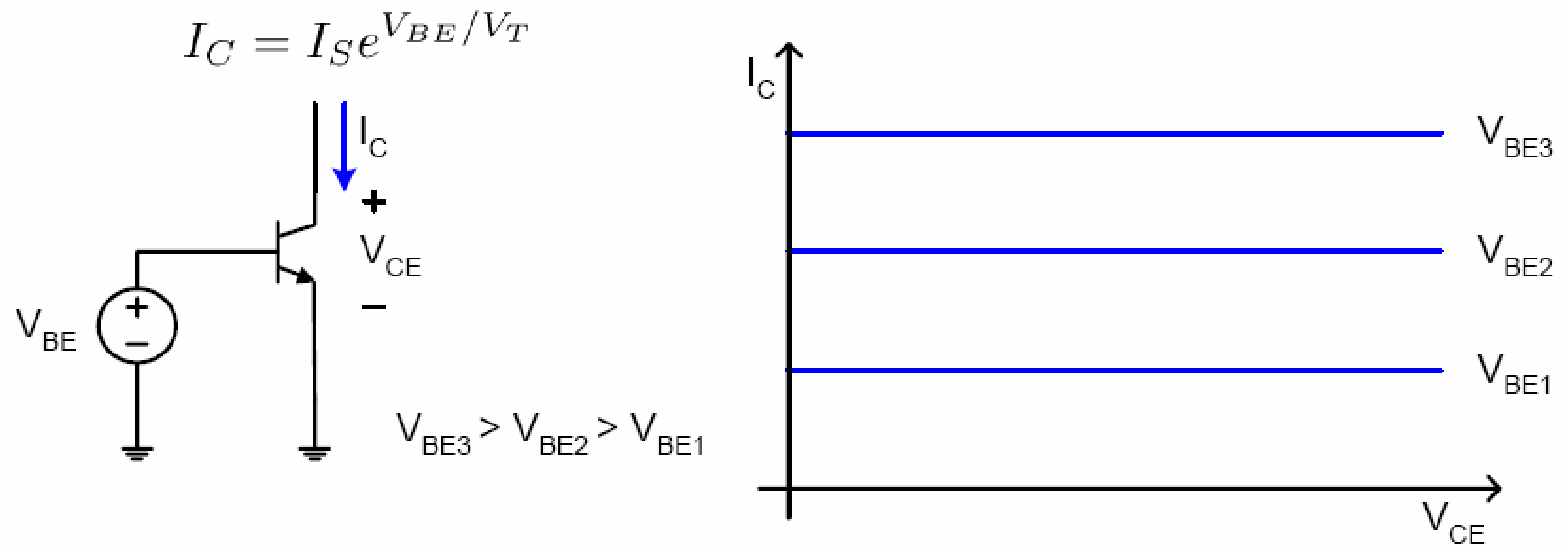
Circuit Symbols and Conventions



pnp transistor structure:



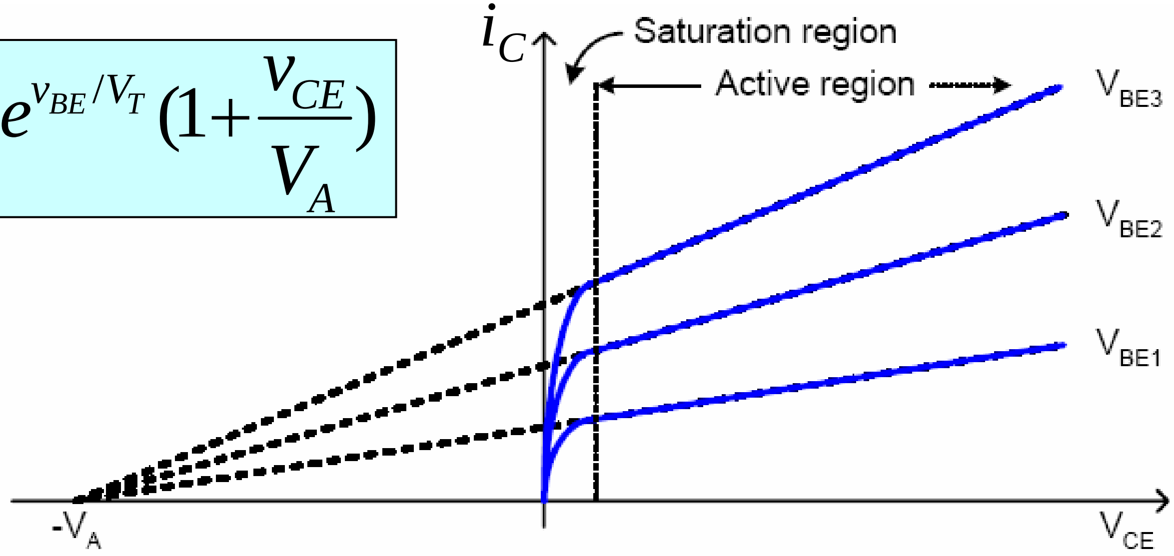
I-V Characteristics



- Collector current vs. v_{CE} shows the BJT looks like a current source (ideally)
  - Plot only shows values where BCJ is reverse biased and so BJT in active region
- However, real BJTs have non-ideal effects

Early Effect

$$i_C = I_S e^{v_{BE}/V_T}\left(1+\frac{v_{CE}}{V_A}\right)$$

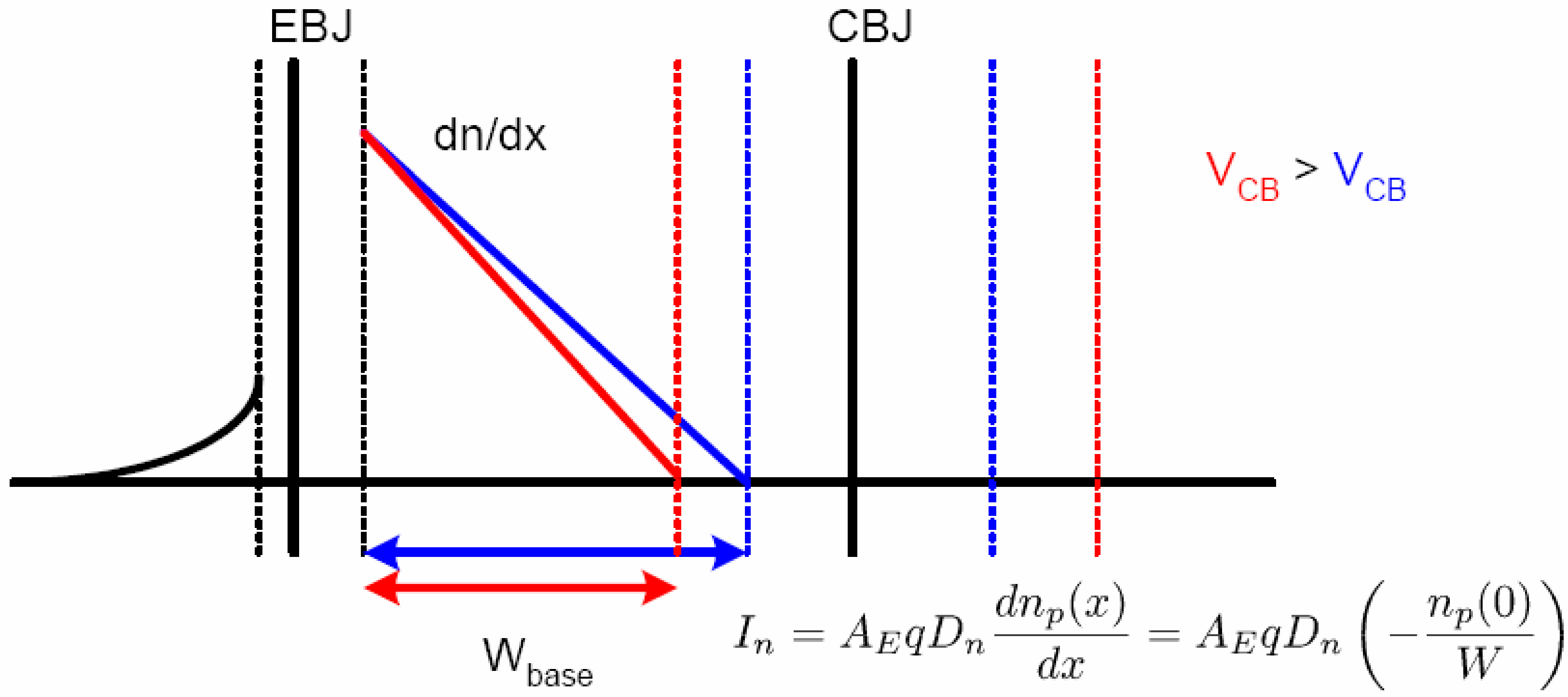


- Early Effect:
  - Current in active region depends (slightly) on v_{CE}
  - Account for Early effect with additional term in collector current equation
  - V_A is a parameter for the BJT (50 to 100) and called the Early voltage
  - Nonzero slope means the output resistance is NOT infinite.

- At low value of v_{CE}, the CBJ becomes forward-biased and the transistor enters the saturation region.

What causes the Early effect?

- When V_{CB} increases:
  - depletion region of CBJ widens
  - so the effective base width decreases (base-width modulation)
- Shorter effective base width → higher dn/dx



$$I_n = A_E q D_n \frac{dn_p(x)}{dx} = A_E q D_n \left(-\frac{n_p(0)}{W}\right)$$

BJT Breakdown

- If reverse voltage across either of the two *pn* junctions in the transistor is too large, corresponding diode will break down.
- Emitter is the most heavily doped region and collector is the most lightly doped region.
- Due to doping differences, base-emitter diode has relatively low breakdown voltage (3 to 10 V). Collector-base diode can be designed to break down at much larger voltages.
- Transistors must be selected in accordance with possible reverse voltages in circuit.

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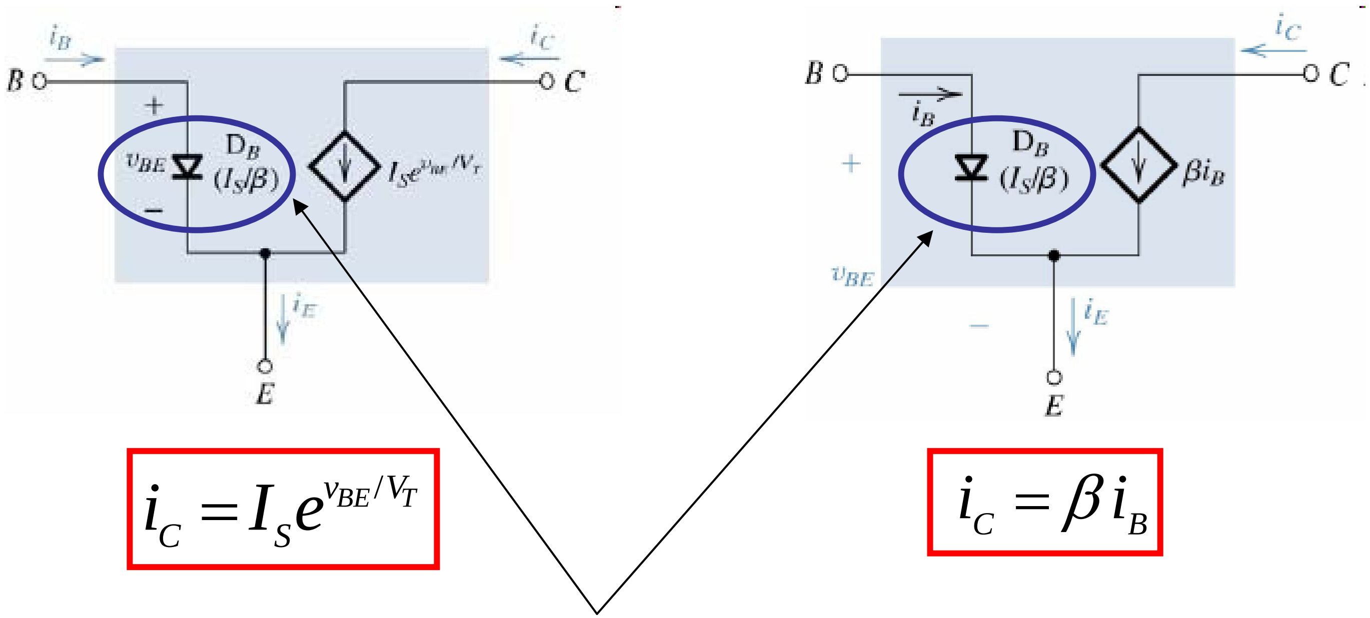
- BJT Circuit Models
- DC Analysis
- BJT Biasing

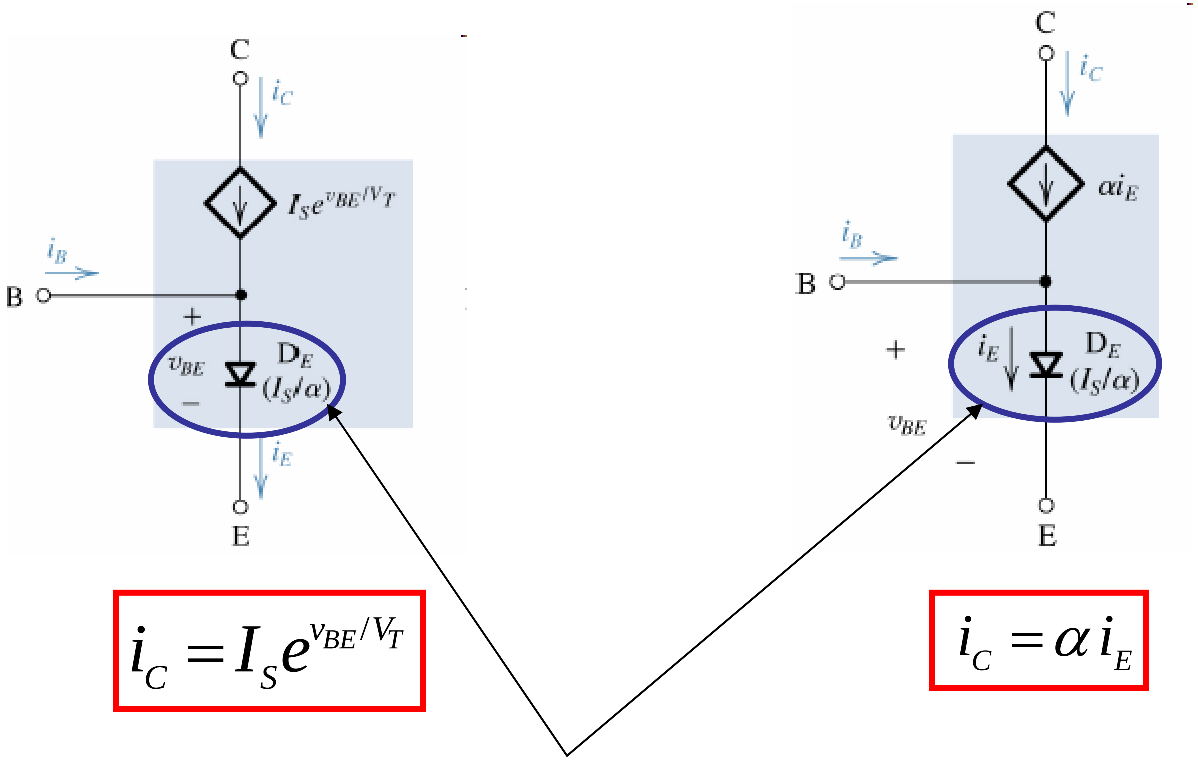
Equivalent Circuits for Active Mode



- Reverse saturation of $D_B = I_S/\beta$, because:

$$i_B = \frac{i_C}{\beta} = \frac{I_S}{\beta} e^{v_{BE}/V_T}$$

Equivalent Circuits for Active Mode



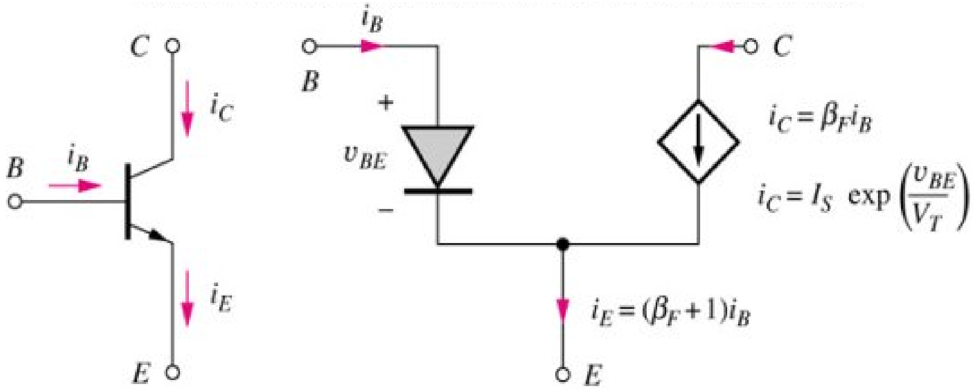
$$i_C = I_S e^{v_{BE}/V_T}$$

$$i_C = \alpha i_E$$

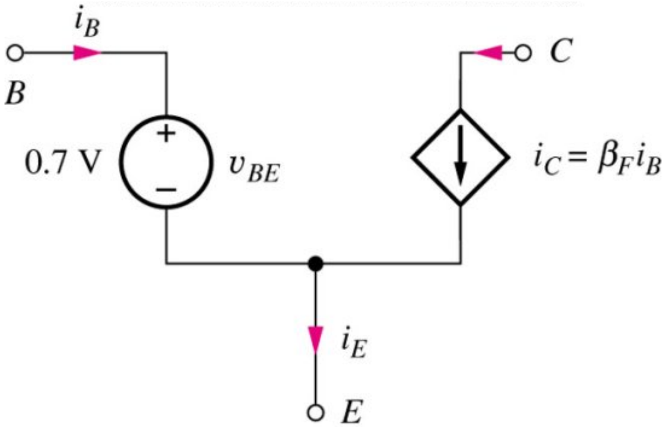
- Reverse saturation of $D_E = I_S/\alpha$, because:

$$i_E = \frac{i_C}{\alpha} = \frac{I_S}{\alpha} e^{v_{BE}/V_T}$$

Simplified Model



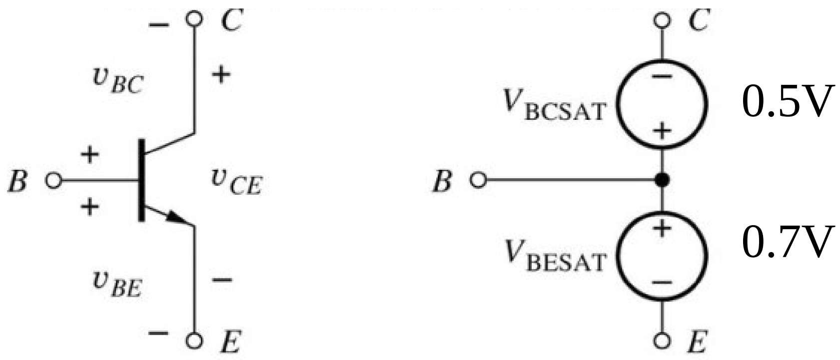
Simplified model:



- Base-emitter diode is replaced by a constant voltage drop (V_{BE} = 0.7 V) since it is biased in forward-active region.

Simplified Circuit Model for Saturation Mode

EBJ Forward-biased; CBJ Forward–biased.



$$V_{CEsat} = 0.2V$$

- Forward voltage drop V_{BC} is small b/c collector doping level is low (by design)

- No expressions for terminal currents other than $i_C + i_B = i_E$.

- The ratio of I_C to I_B is called the forced current gain,

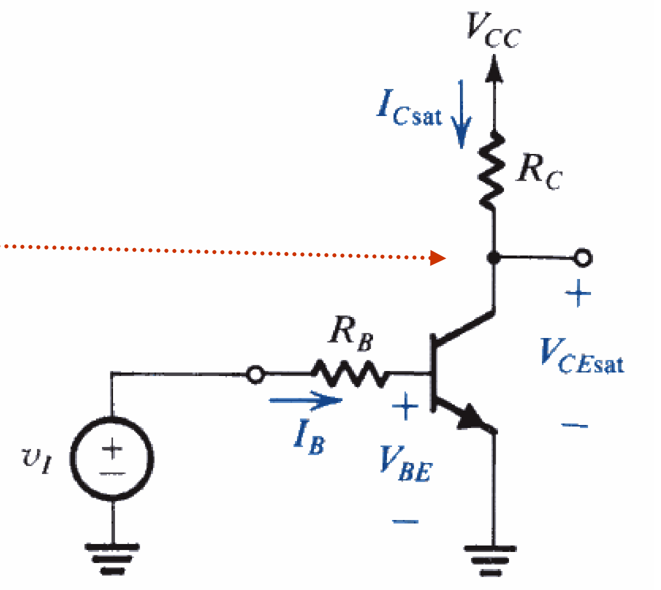
$$\hat{\beta} = I_{Csat} / I_{Bsat}$$

which is much smaller than β → next slide.

Forced Beta

Assume BJT works in active mode:

- Increase I_B (or V_I) causes
  - I_C to increase proportionally ($I_C = \beta I_B$)
  - V_C to drop



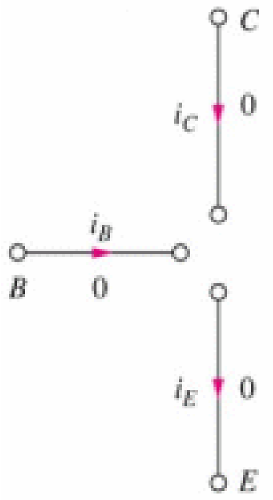
- V_C will drop to a point where BCJ becomes forward-biased, then:
  - V_{CE} clamps to V_{BE} - 0.5V, or 0.2V
  - Further increases of I_B will not increase I_C
  - I_C is said "***saturated***"
  - I_C/I_B becomes smaller than β and is called "forced β".

Simplified Circuit Model for Cutoff Mode

Cutoff Region:

EBJ Reverse-biased
CBJ Reverse-biased

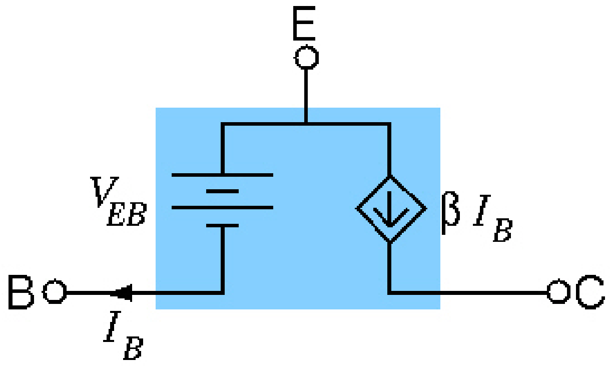
$$i_B = 0, \quad i_E = 0, \quad i_C = 0:$$



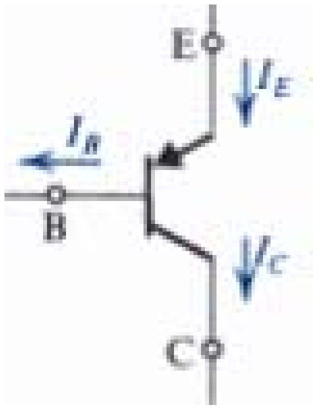
No expression for terminal voltages.

Models for *pnp* Transistors

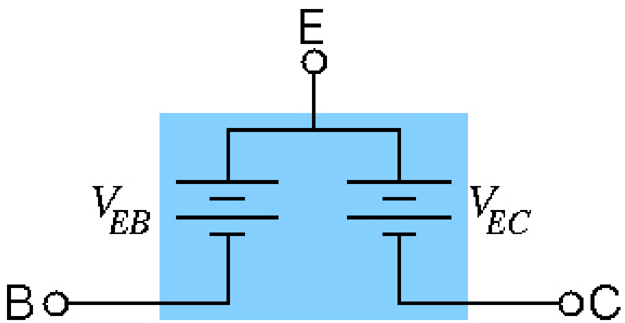
PNP model in active mode



$V_{EB} \cong 0.7\ \text{V}$



PNP model in saturation mode



$V_{EB} \cong 0.7\ \text{V}$

$V_{EC} \cong 0.2\ \text{V}$

Topics to cover …

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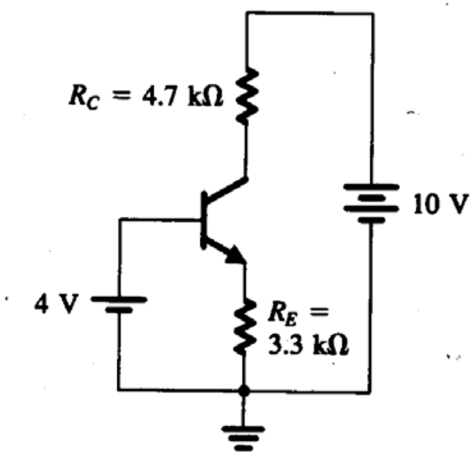
- DC Analysis
- BJT Biasing

Example 1



- **Problem:** Determine the Q-point.
- **Given data:** β **=** 100
- **Assumptions:** V_{BE} = 0.7 V
- **Analysis:**

Assume active mode of operation,

$$V_E = 4 - V_{BE} \cong 4 - 0.7 = 3.3\,\text{V}$$

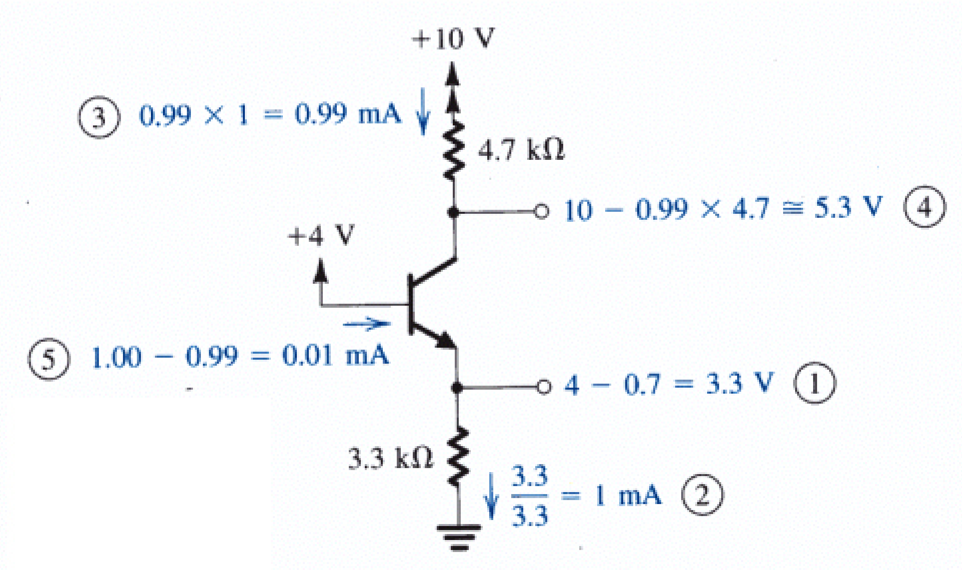
$$I_E = \frac{V_E}{R_E} = \frac{3.3}{3.3} = 1\,\text{mA}$$

For active mode operation, $I_C = \alpha I_E$

$$\because \alpha = \frac{\beta}{\beta+1} = \frac{100}{101} \cong 0.99$$

$$\therefore I_C = 0.99 \times 1 = 0.99\,\text{mA}$$

$$V_C = 10 - I_C R_C = 10 - 0.99 \times 4.7 \cong +5.3\,\text{V}$$



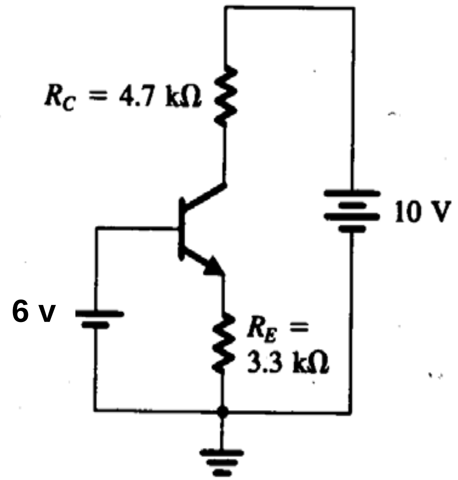
V_{BC}= –1.3 V. The CBJ is reverse-biased and the transistor is indeed in the active mode as assumed.

$$I_B = \frac{I_E}{\beta+1} = \frac{1}{101} \cong 0.01\,\text{mA}$$

Example 2

- **Problem:** V_B changes to 6V. Find Q-point.
- **Analysis:**

Assume active mode operation, we have



$$V_E = 6 - V_{BE} \cong 6 - 0.7 = 5.3\,\text{V}$$

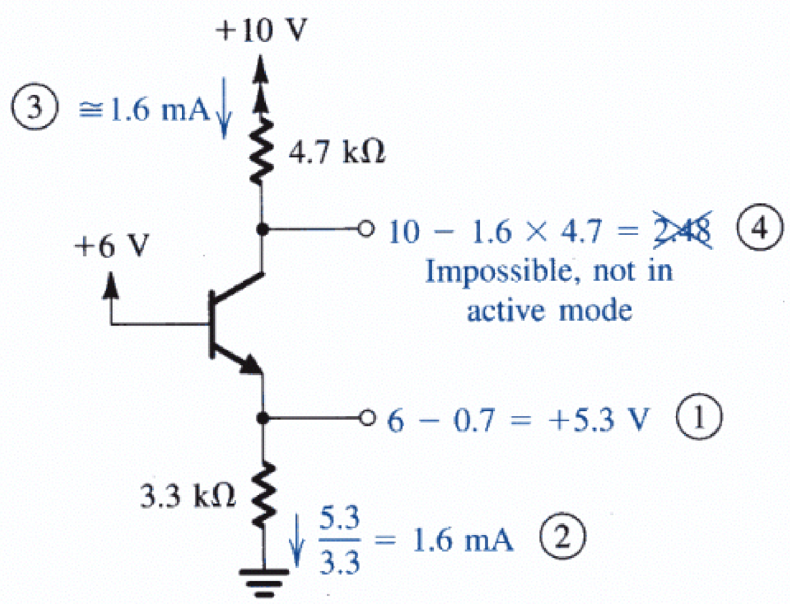
$$I_E = \frac{V_E}{R_E} = \frac{5.3}{3.3} = 1.6\,\text{mA}$$

For active mode operation,

$$I_C = \alpha I_E = 0.99 \times 1.6 \cong 1.6\,\text{mA}$$

$$V_C = 10 - I_C R_C = 10 - 1.6 \times 4.7 \cong +2.48\,\text{V}$$

Since V_{BC}= 6 – 2.48 = 3.52 V, the CBJ is forward-biased and the original assumption of active mode operation is INCORRECT. A Second guess must be tried.



Example 2 (Cont.)

Assume the transistor is in saturation region.
Use the saturation model, we have

$$V_E = 6 - V_{BE} \cong 6 - 0.7 = 5.3\,\text{V}$$

$$I_E = \frac{V_E}{R_E} = \frac{5.3}{3.3} = 1.6\,\text{mA}$$

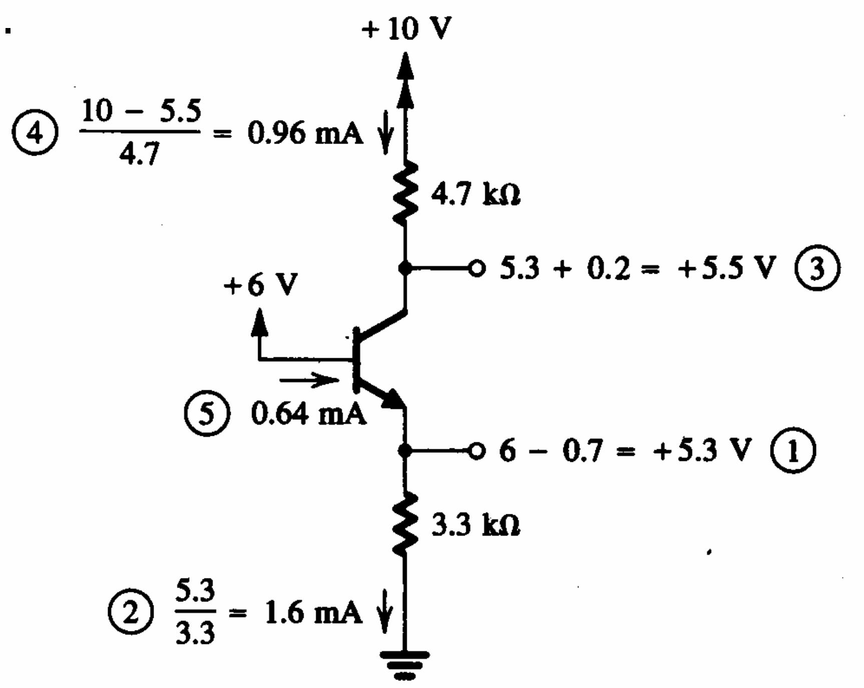
$$V_C = V_E + V_{CEsat} \cong +5.3 + 0.2 = 5.5\,\text{V}$$

$$I_C = \frac{10 - 5.5}{4.7} = 0.96\,\text{mA}$$

$$I_B = I_E - I_C = 1.6 - 0.96 = 0.64\,\text{mA}$$

Thus the transistor is operating at a forced β of

$$\beta_{\text{forced}} = \frac{I_C}{I_B} = \frac{0.96}{0.64} = 1.5$$



Since β_{forced} << normal β of 100, the transistor is indeed saturated.

Example 3

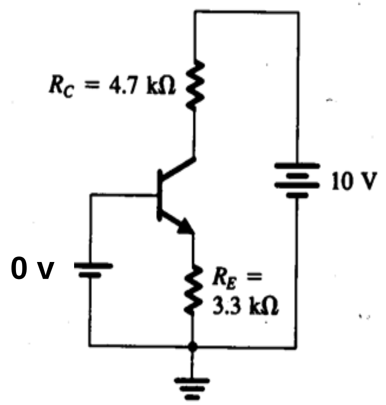
- **Problem:** V_B changes to 0V. Find Q-point.
- **Analysis:**

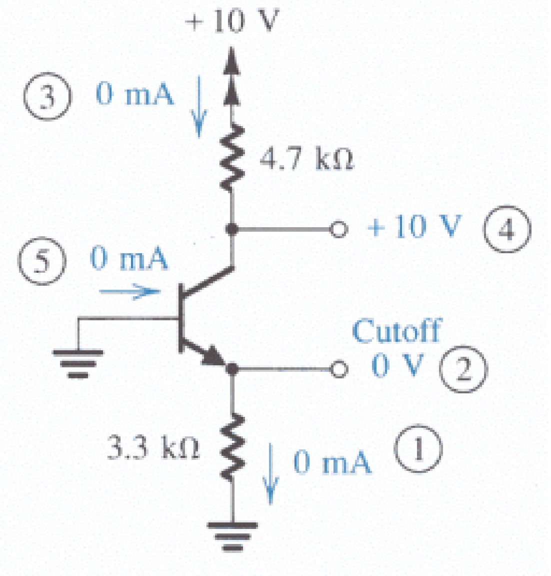
Assume the transistor operates in cut-off mode:

$$i_B = 0, \quad i_E = 0, \quad i_C = 0$$
$$v_C = V_{CC}$$

V_{BE}=0 V: BEJ reverse-biased
V_{BC}=-10V: BCJ reverse-biased

Assumption is correct.





Summary: BJT DC Analysis

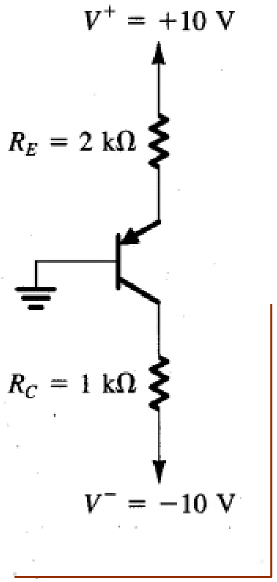
1. Assume the BJT is biased in the active mode in which case $V_{BE} = V_{BE}(on)$, $I_B>0$ and $I_C=\beta I_B$.

2. Analyze the "linear" circuit with the active-mode equivalent circuit.

3. Evaluate the resulting state of the BJT. If reverse-biasing of BCJ ($V_{CE}>V_{CE}(sat)$) and forward-biasing of BEJ ($I_B>0$) are true, then the initial assumption is correct. However,
   – If $I_B < 0$, then the BJT is probably cutoff,
   – If $V_{CE}<V_{CE}(sat)$, it is likely in saturation.

4. If the initial assumption is proven incorrect, then a new assumption must be made and the new "linear" circuit must be analyzed. Step 3 must then be repeated.

Example 4



- **Problem:** Determine the Q-point
- **Given data:** β **=** 100
- **Assumptions:** V_{BE} = 0.7 V
- **Analysis:**

EBJ must be forward-biased.

$$V_E = V_{EB} \cong 0.7 \text{ V}$$

$$I_E = \frac{V^+ - V_E}{R_E} = \frac{10-0.7}{2} = 4.65 \text{ mA}$$

Assume active-mode operation, we have

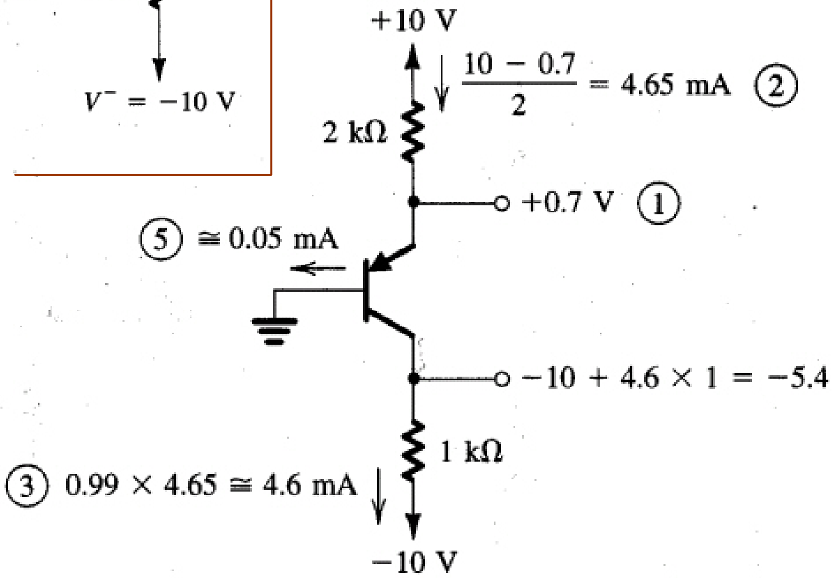
$$I_C = \alpha I_E \text{ and } \alpha = \frac{\beta}{\beta+1} = 0.99$$

$$I_C = 0.99 \times 4.65 = 4.6 \text{ mA}$$

$$V_C = V^- + I_C R_C = -10 + 4.6 \times 1 = -5.4 \text{ V}$$

Thus V_{BC}= 5.4 V. The CBJ is reverse-biased and the transistor is indeed in the active mode as assumed.

$$I_B = \frac{I_E}{\beta+1} = \frac{4.65}{101} \cong 0.05 \text{ mA}$$



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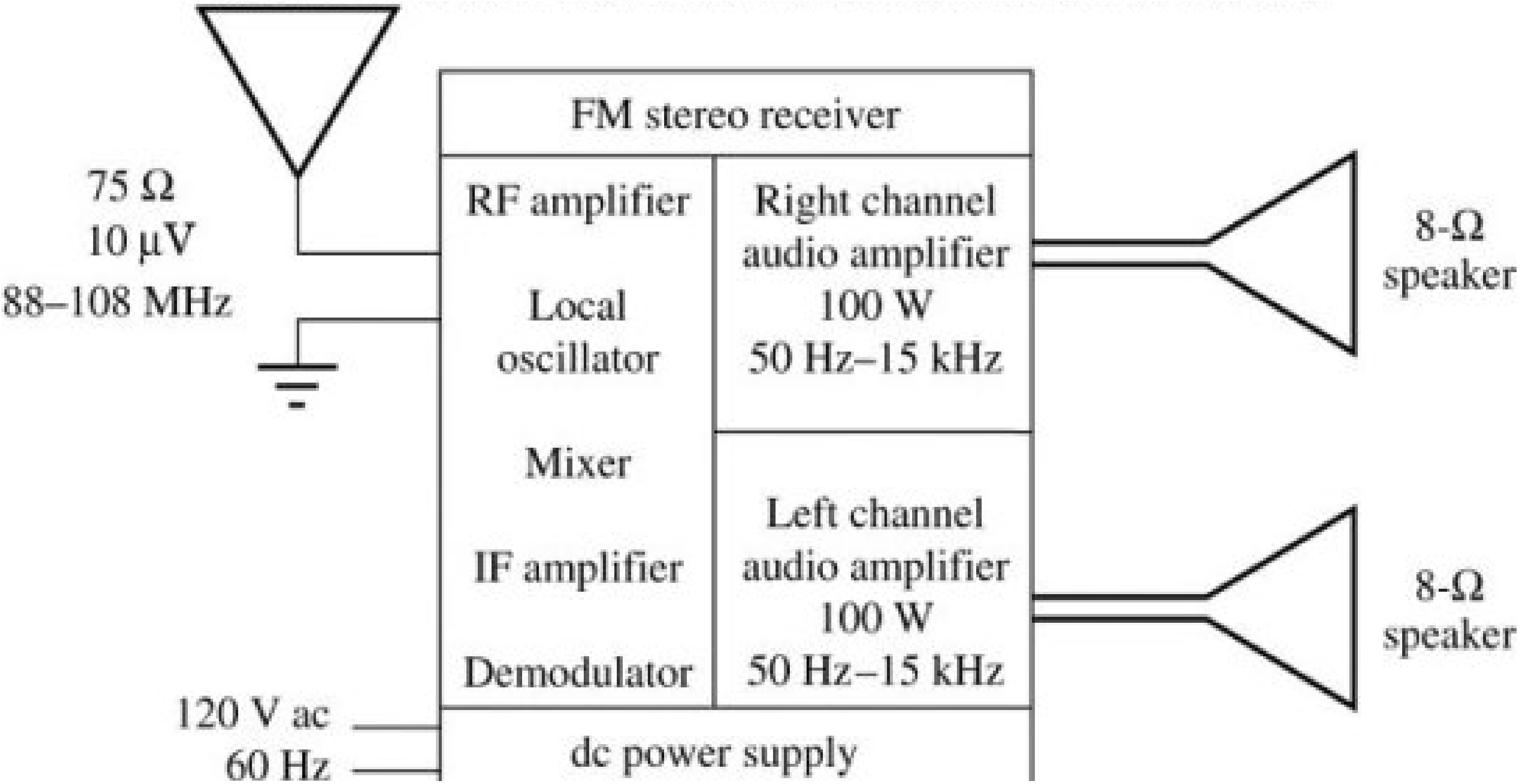
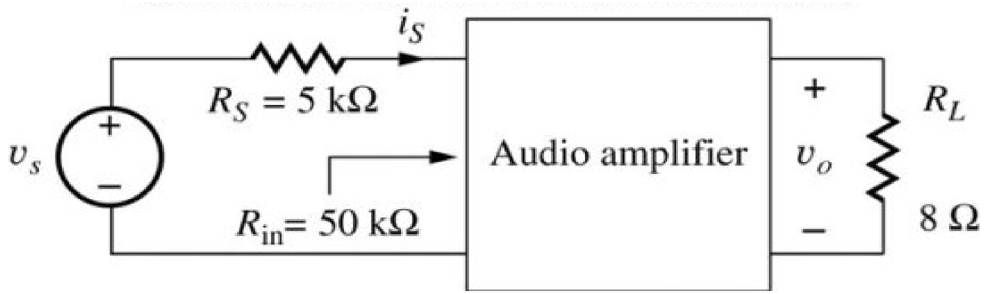
Example of Analog Electronic System: FM Stereo Receiver



Amplification: Introduction



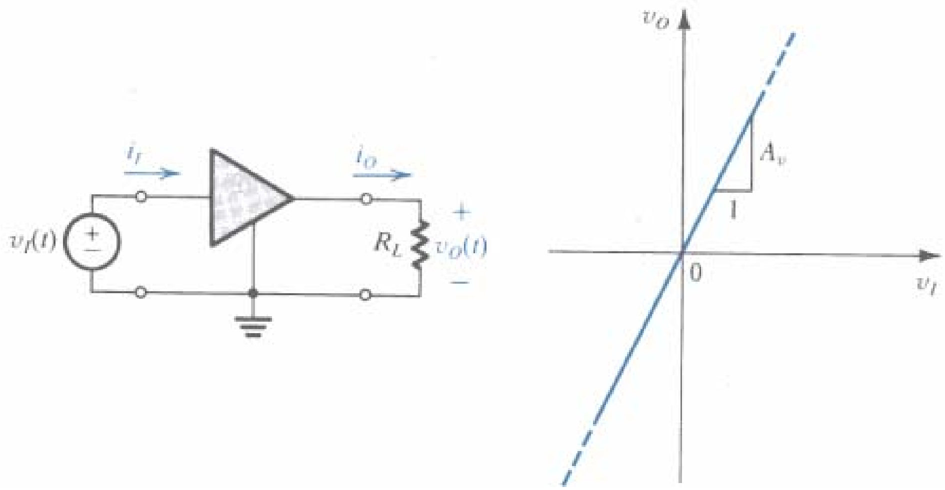
A periodic signal can be represented as the sum of many individual sine waves. We consider only one component with amplitude V_S=1 mV and frequency ω_S with 0 phase (signal is used as the reference):

$$v_S = V_S \sin \omega_S t$$

Amplifier output is sinusoidal with same frequency but different amplitude V_O and phase θ:

$$v_O = V_O (\sin \omega_S t + \theta)$$

Transfer characteristic of the ideal amplifier



$$\text{Voltage gain } (A_v) \equiv \frac{v_O}{v_I}$$

$$\text{Current gain } (A_i) \equiv \frac{i_O}{i_I}$$

$$\text{Power gain } (A_p) \equiv \frac{\text{load power } (P_L)}{\text{input power } (P_I)}$$

Historically, electronic engineers are used to express gain with a logarithmic measure as:

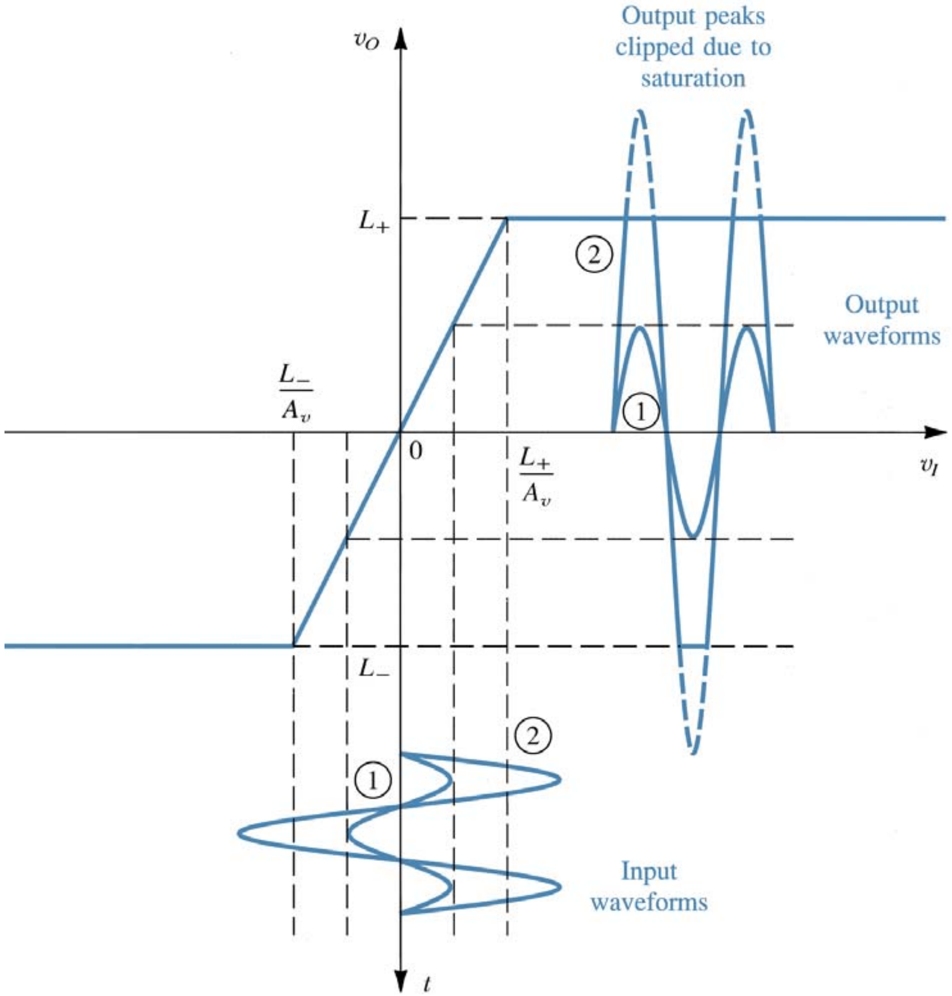
$$\text{Voltage gain in decibels} = 20 \log |A_v| \text{ dB}$$

$$\text{Current gain in decibels} = 20 \log |A_i| \text{ dB}$$

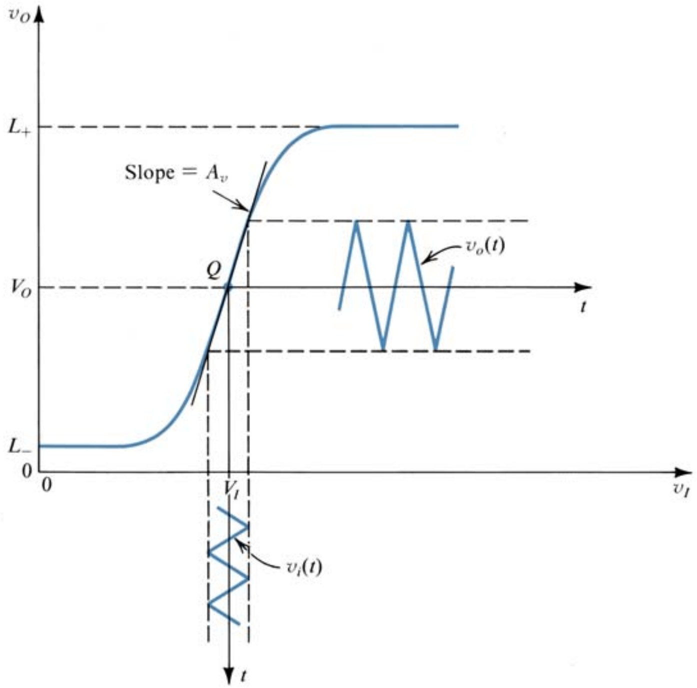
$$\text{Power gain in decibels} = 10 \log A_p \text{ dB}$$

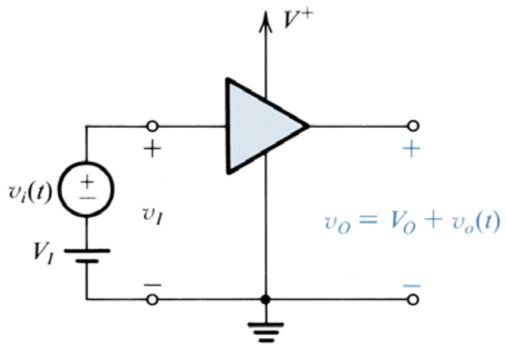
Amplifier Saturation

- The amplifier remains linear over only a limited range of input and output.



The concept of Biasing





- The transfer characteristic of a practical amplifiers may not have a linear segment around the origin.
- To obtain linear amplification, one can bias the circuit to operate at a point near the middle of the linear segment. The point Q is known as the ***quiescent point***, the ***dc bias point***, or simply the ***operating point***.

$$v_I(t) = V_I + v_i(t)$$

$$v_O(t) = V_O + v_o(t) \quad \text{with} \quad v_o(t) = A_v v_i(t)$$

$$\text{where} \qquad A_v = \left.\frac{dv_O}{dv_I}\right|_{at\ Q}$$

- The input signal must be kept sufficiently small.

Transfer Characteristic of BJT Amplifier: Example 5

- **Problem:** Determine the dc voltage transfer characteristic of the circuit for 0 < v_I <5 V
- **Analysis:**

For $v_I \le 0.7$ V, Q is cut off and $v_O = 5$ V.

For $v_I > 0.7$ V, Q turns on and is in the active mode, so that

$$i_B = \frac{v_I - V_{BE}}{R_B} = \frac{v_I - 0.7}{100\text{k}\Omega}$$

The output voltage is

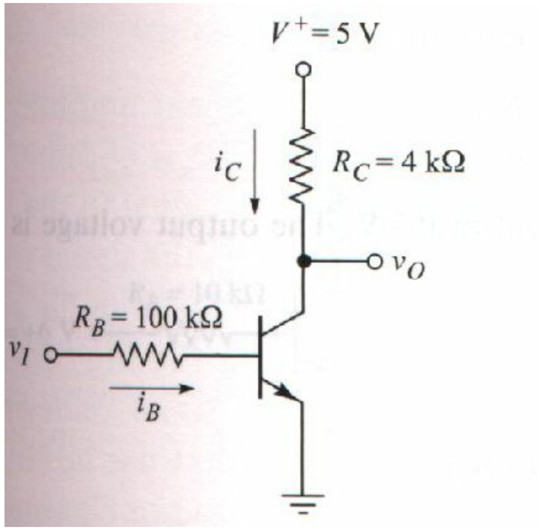
$$v_O = V^+ - i_C R_C = V^+ - \beta i_B R_C$$

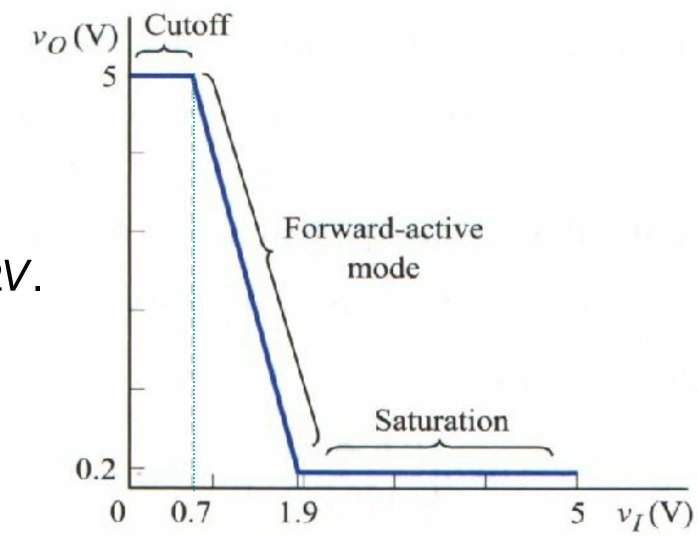
or

$$v_O = 5 - (100)\left[\frac{v_I - 0.7}{100\text{k}\Omega}\right]4\text{k}\Omega$$

This equation is valid for $v_I \ge 0.7$ V and $v_O \ge v_{CE}(\text{sat}) = 0.2V$.

The input voltage for $v_O = 0.2$ V is found to be $v_I = 1.9$ V.
Now, for $v_I > 1.9$ V, the transistor is in saturation.





Conceptual Bias Circuit for BJT

- In order to create a linear amplifier, we must keep the transistor in the active mode, establish a Q-point near the center of the active region, and couple the time-varying signal to the base.