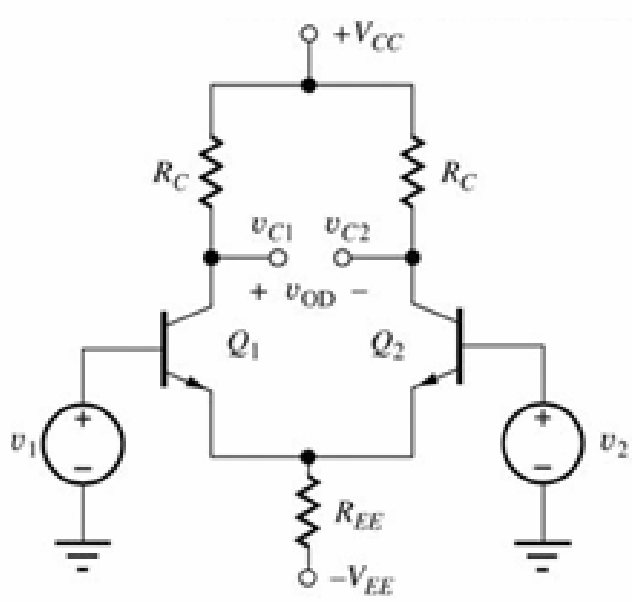
Week 11: Differential Amplifiers

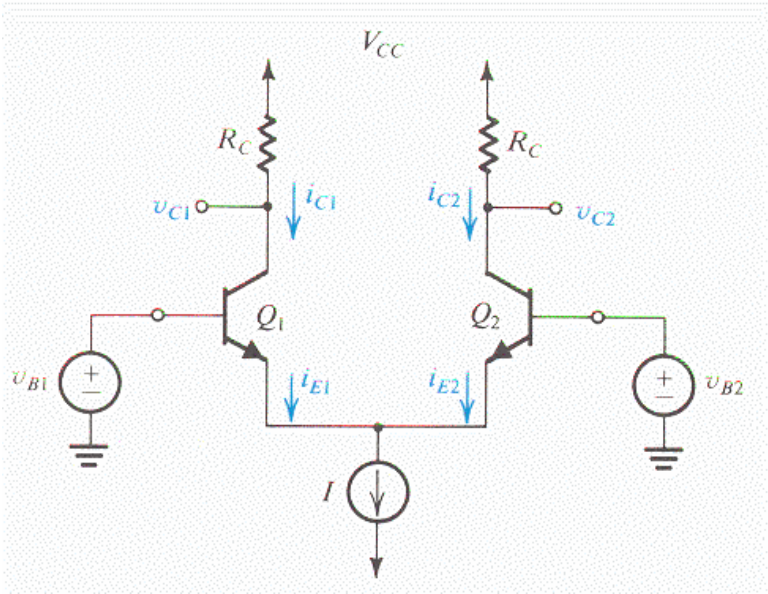
Topics to cover …

- Large signal analysis
- AC analysis
- Half-circuit analysis

Reading Assignment:
Chap 15.1-15.8 of Jaeger and Blalock or
Chap 7.1 - 7.3, of Sedra and Smith

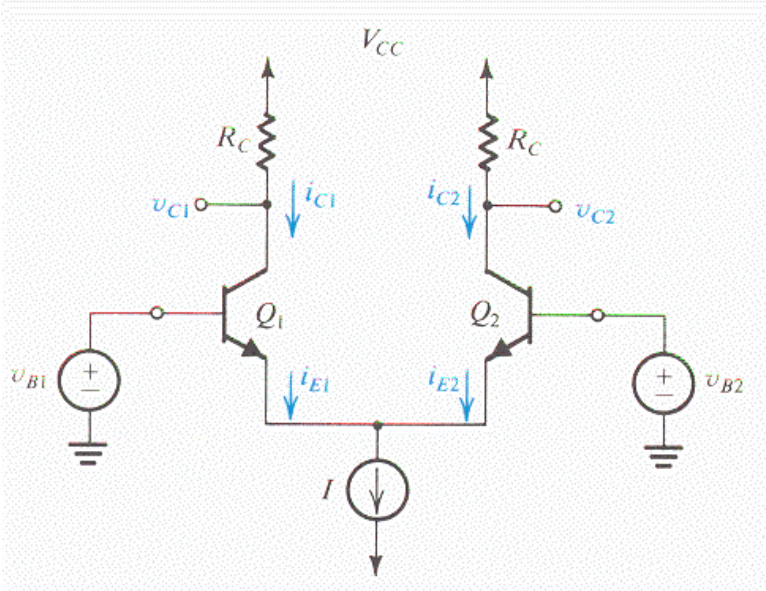
BJT Differential Pair





- Two identical transistors with emitters shorted together, connecting to a resistor or a current source. Transistors operate in active mode.
- Designed to amplify voltage difference between the two inputs
- One of the most used circuit building blocks
  - E.g., as the input stage of opamps

Large Signal Analysis



$$I = i_{E1} + i_{E2} = i_{C1}/\alpha + i_{C2}/\alpha$$

$$\Rightarrow \frac{\alpha I}{i_{C1}} = \frac{i_{C2}}{i_{C1}} + 1 \qquad i_{C1} = \frac{\alpha I}{1 + e^{-v_{id}/V_T}}$$

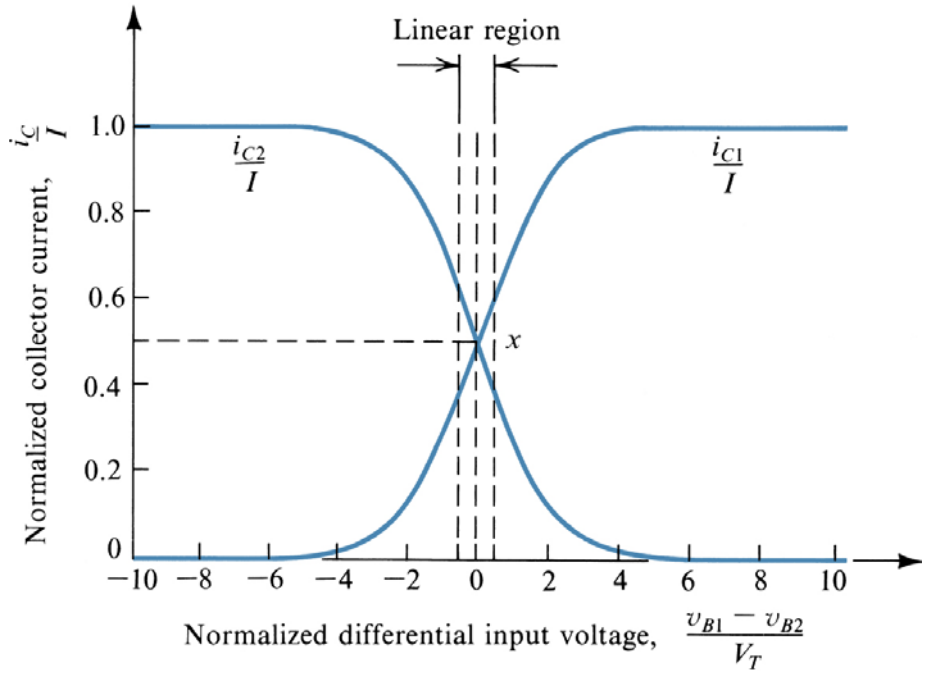
$$\Rightarrow i_{C1} = \frac{\alpha I}{\frac{i_{C2}}{i_{C1}} + 1} \qquad i_{C2} = \frac{\alpha I}{1 + e^{+v_{id}/V_T}}$$

$$i_{C1} = I_S e^{v_{BE1}/V_T}$$

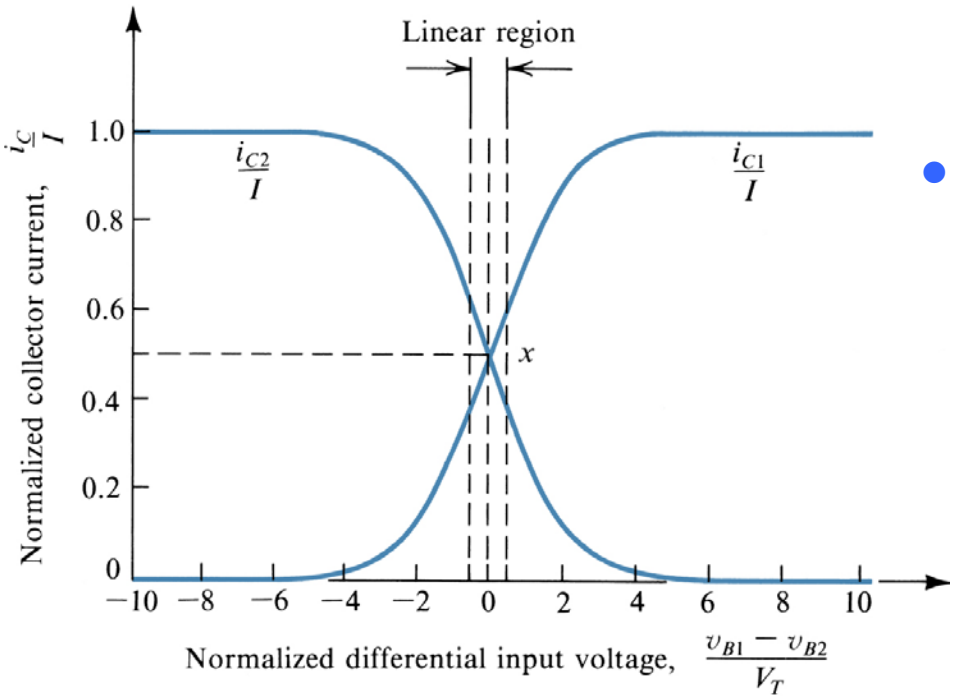
$$i_{C2} = I_S e^{v_{BE2}/V_T}$$

$$i_{C1}/i_{C2} = e^{(v_{BE1} - v_{BE2})/V_T} = e^{v_{id}/V_T}$$

where $v_{BE1} - v_{BE2} = v_{B1} - v_{B2} = v_{id}$

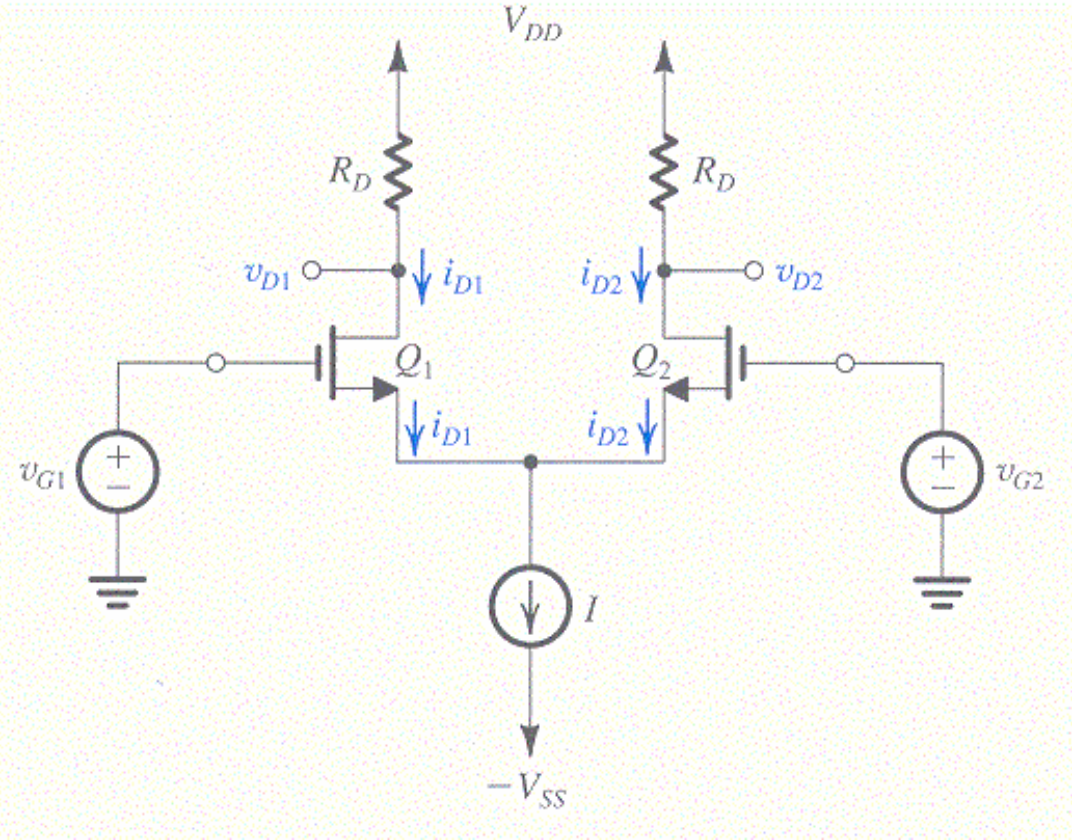


Large Signal Analysis



- $|v_d| = |v_{B1}-v_{B2}| < V_T$ for use as a linear amplifier
- For $|v_d| > 4V_T$ (≈100mV), the tail current flows almost entirely in one of the two transistors
  - This high sensitivity makes the differential pair a fast current switch
  - The transistors are either in active mode or in cutoff mode
    - Also contributes to high switching speed

MOS Differential Pair



Large Signal Analysis

Assuming identical devices and neglecting the output resistance and body effect, the drain currents are

$$\begin{cases} i_{D1} = \frac{1}{2} k_n' \frac{W}{L} (v_{GS1} - V_t)^2 \\ i_{D2} = \frac{1}{2} k_n' \frac{W}{L} (v_{GS2} - V_t)^2 \end{cases}$$

$$\begin{cases} \sqrt{i_{D1}} = \sqrt{\frac{1}{2} k_n' \frac{W}{L}} (v_{GS1} - V_t) \\ \sqrt{i_{D2}} = \sqrt{\frac{1}{2} k_n' \frac{W}{L}} (v_{GS2} - V_t) \end{cases}$$

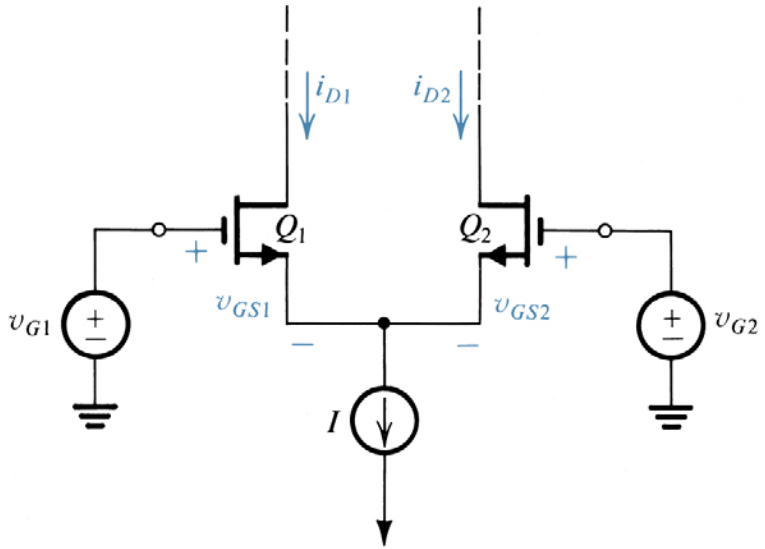


Fig. 6.29 The MOSFET differential pair.

Since, $v_{GS1} - v_{GS2} = v_{id}$

We have $$\sqrt{i_{D1}} - \sqrt{i_{D2}} = \sqrt{\frac{1}{2} k_n' \frac{W}{L}} v_{id} \quad (1)$$

The current-source bias imposes the constrain

$$i_{D1} + i_{D2} = I \quad (2)$$

Solving eqs (1) & (2) yields

$$\begin{cases} i_{D1} = \frac{I}{2} + \sqrt{k_n' \frac{W}{L} I} \left(\frac{v_{id}}{2} \right) \sqrt{1 - \frac{(v_{id}/2)^2}{I / k_n' \frac{W}{L}}} \\ i_{D2} = \frac{I}{2} - \sqrt{k_n' \frac{W}{L} I} \left(\frac{v_{id}}{2} \right) \sqrt{1 - \frac{(v_{id}/2)^2}{I / k_n' \frac{W}{L}}} \end{cases}$$

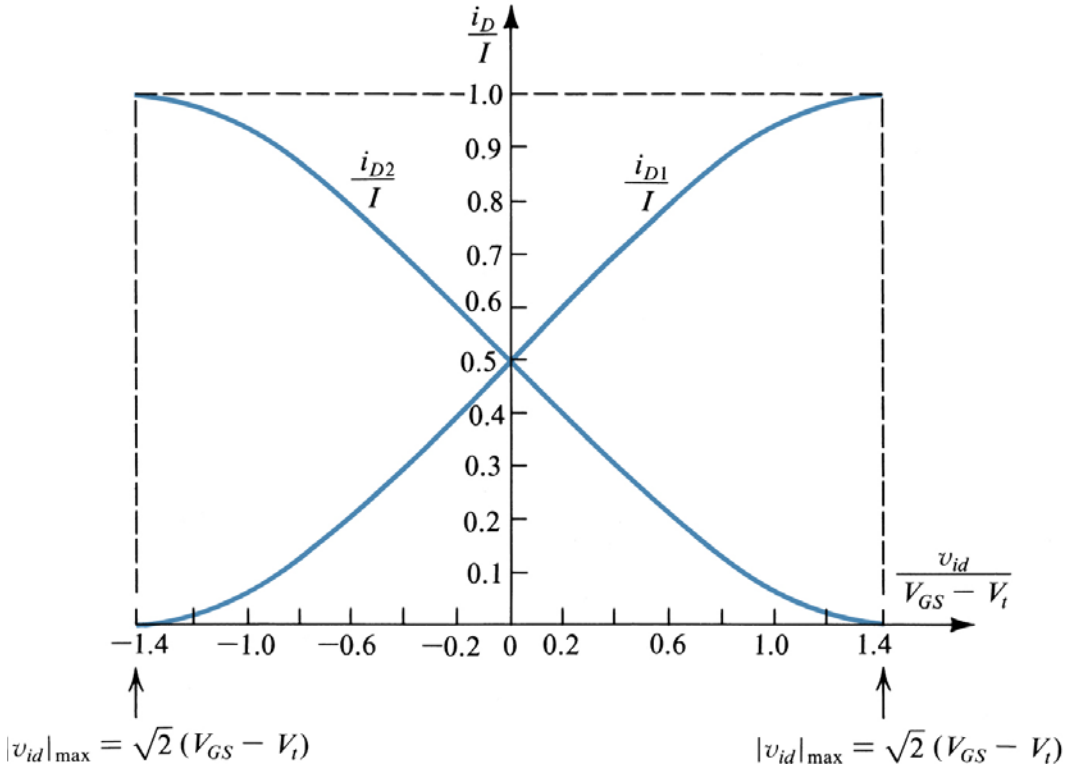
Large Signal Analysis

At the bias point, $v_{id} = 0$, leading to $i_{D1} = i_{D2} = \frac{I}{2}$

Correspondingly, $v_{GS1} = v_{GS2} = V_{GS}$

where $\frac{I}{2} = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_t)^2$

$$\therefore \begin{cases} i_{D1} = \frac{I}{2} + \frac{I}{V_{GS} - V_t} \left(\frac{v_{id}}{2} \right) \sqrt{1 - \left(\frac{v_{id}/2}{V_{GS} - V_t} \right)^2} \\ i_{D2} = \frac{I}{2} - \frac{I}{V_{GS} - V_t} \left(\frac{v_{id}}{2} \right) \sqrt{1 - \left(\frac{v_{id}/2}{V_{GS} - V_t} \right)^2} \end{cases}$$



Large Signal Analysis

For $v_{id}/2 << V_{GS} - V_t$ (small signal approximation)

$$\begin{cases} i_{D1} = \dfrac{I}{2} + \dfrac{I}{V_{GS} - V_t}\left(\dfrac{v_{id}}{2}\right) \\ i_{D2} = \dfrac{I}{2} - \dfrac{I}{V_{GS} - V_t}\left(\dfrac{v_{id}}{2}\right) \end{cases}$$

Since $g_m = \dfrac{2(I/2)}{V_{GS} - V_t} = \dfrac{I}{V_{GS} - V_t}$

We have the signal component i_d of i_D as $\boxed{i_d = g_m(v_{id}/2)}$

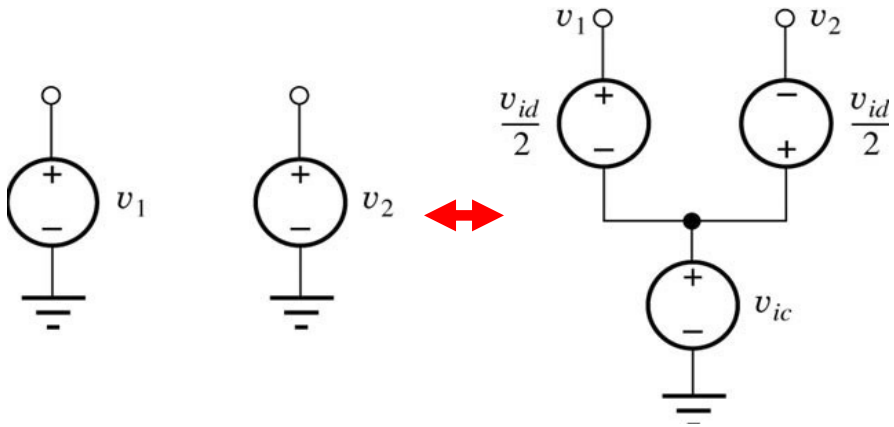
At full switching situation (that is, i_{D1}=I and i_{D2}=0, or vice versa), the value of v_{id} is:

$$|v_{id}|_{\max} = \sqrt{2}(V_{GS} - V_t)$$

Topics to cover …

- Large signal analysis
- AC analysis
- Half-circuit analysis

Modeling Inputs



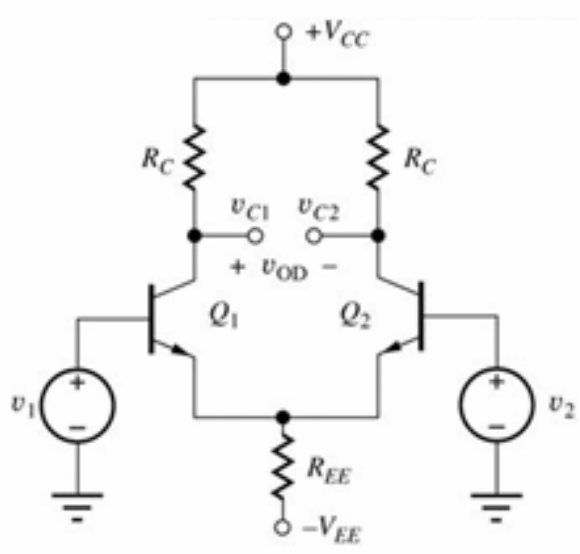
Common-mode component:
(the average)

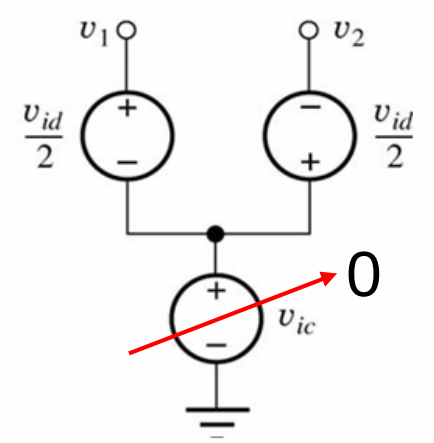
$$v_{ic} = \frac{v_1 + v_2}{2}$$

Differential-mode component:
(the difference)

$$v_{id} = v_1 - v_2$$

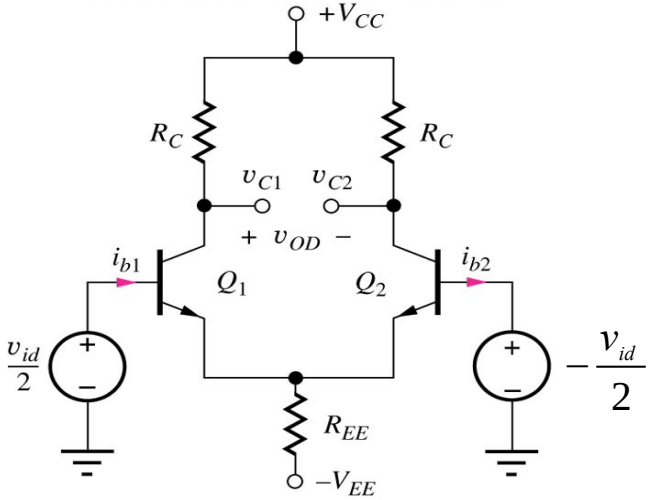
Differential Mode Input



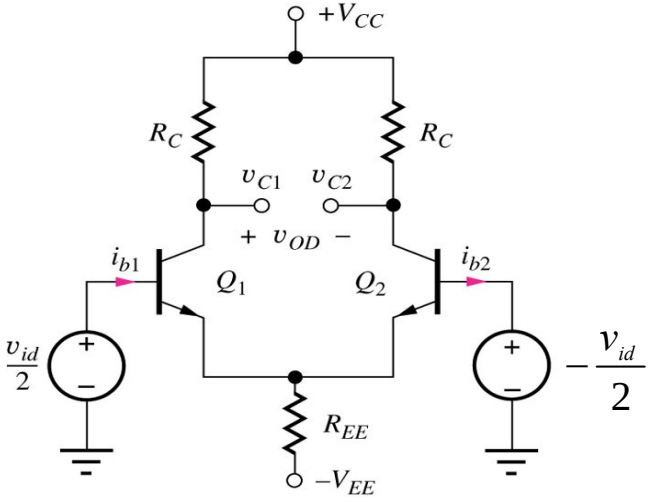


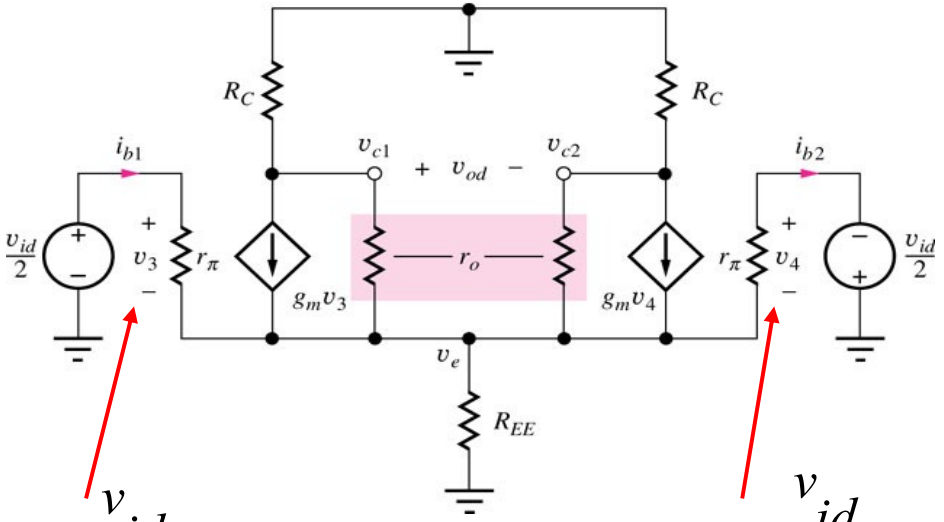
Analyze the circuit by
superposition of DM and CM signals

First set the common-mode input to 0:



AC Analysis for Differential-Mode Input





$$v_3 = \frac{v_{id}}{2} - v_e \qquad v_4 = -\frac{v_{id}}{2} - v_e$$

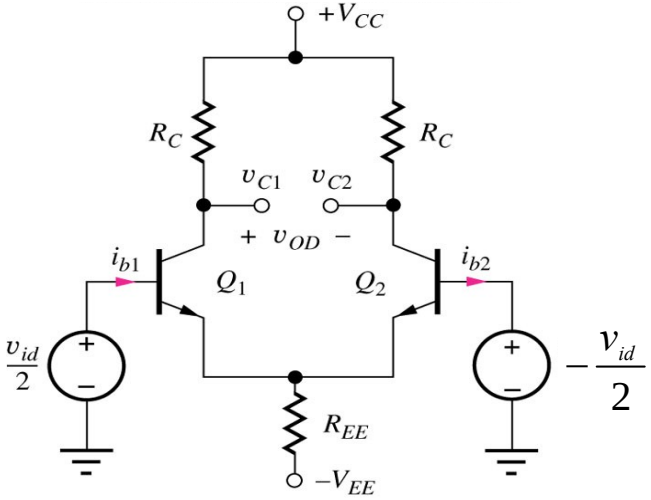
Ignoring r_o, we have $g_m v_3 + \frac{v_3}{r_\pi} + g_m v_4 + \frac{v_4}{r_\pi} = \frac{v_e}{R_{EE}}$ → $(g_m + \frac{1}{r_\pi})(v_3 + v_4) = \frac{v_e}{R_{EE}}$

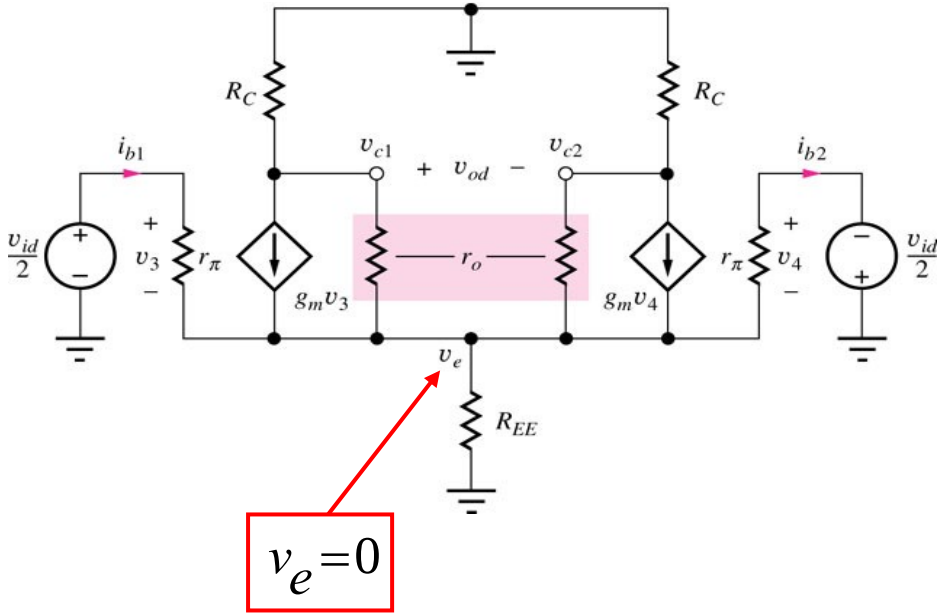
→ $(g_m + \frac{1}{r_\pi})(-2v_e) = \frac{v_e}{R_{EE}}$ → $\boxed{v_e = 0}$

Emitter = AC ground for DM input.

No bypass cap is needed!

Voltage Gain for Differential Output





$$\therefore v_3 = v_{id}/2 \qquad v_4 = -v_{id}/2$$

$$v_{c1} = -g_m R_C \frac{v_{id}}{2} \qquad v_{c2} = +g_m R_C \frac{v_{id}}{2}$$

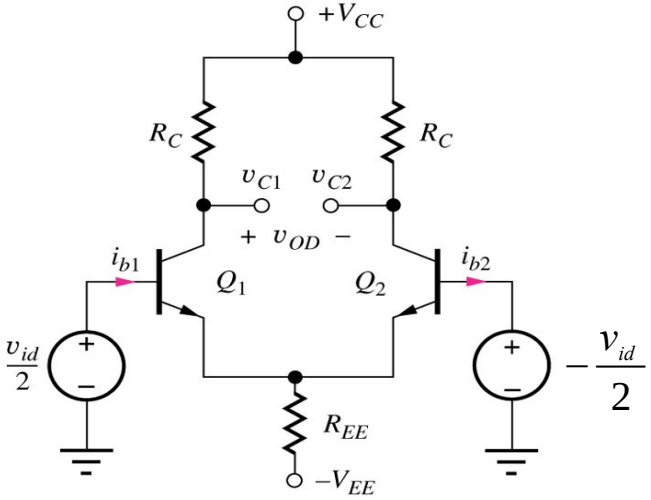
Differential output:

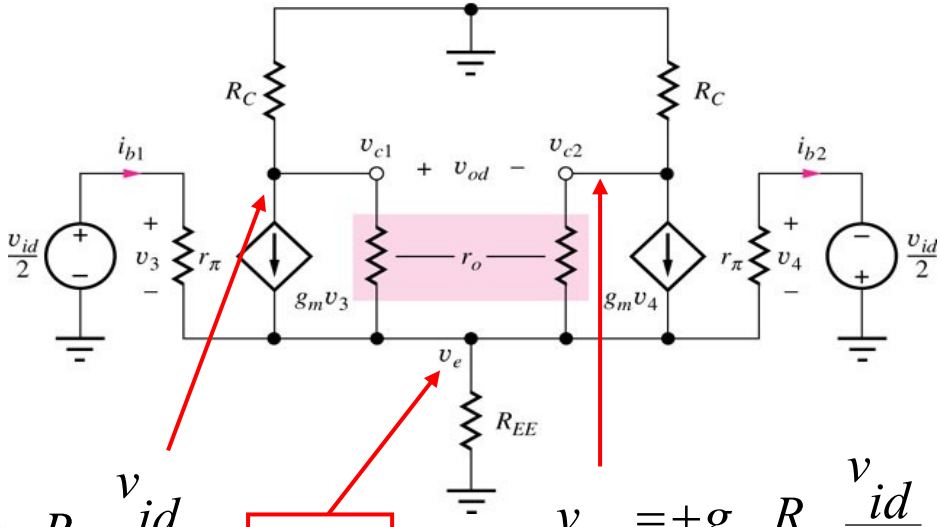
$$v_{od} = v_{c1} - v_{c2} = -g_m R_C v_{id}$$

Differential-mode gain is:

$$A_{dd} \equiv \left. \frac{v_{od}}{v_{id}} \right|_{v_{ic}=0} = -g_m R_C$$

Voltage Gain for Single-ended Output





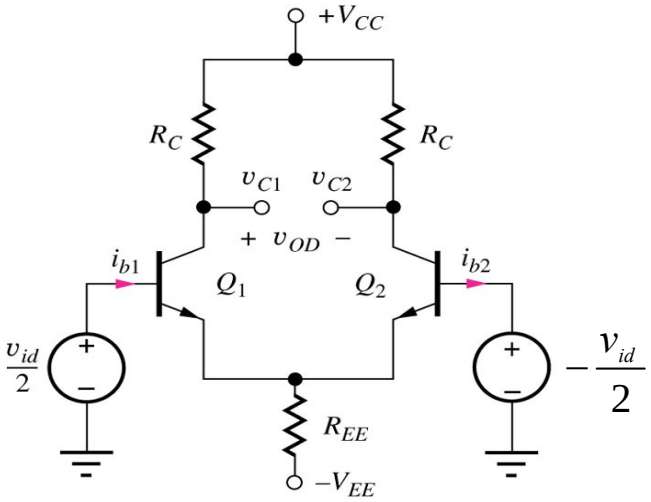
$$v_{c1} = -g_m R_C \frac{v_{id}}{2} \qquad v_e = 0 \qquad v_{c2} = +g_m R_C \frac{v_{id}}{2}$$

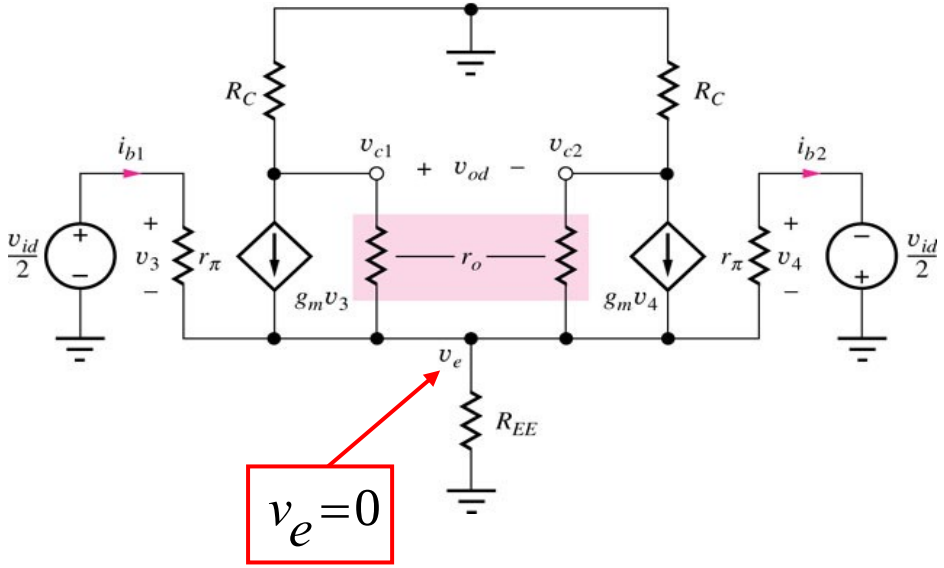
If either v_{c1} or v_{c2} is used alone as output, output is said to be ***single-ended***.

$$A_{dd1} \equiv \left.\frac{v_{c1}}{v_{id}}\right|_{v_{ic}=0} = -\frac{g_m R_C}{2} = \frac{A_{dd}}{2}$$

$$A_{dd2} \equiv \left.\frac{v_{c2}}{v_{id}}\right|_{v_{ic}=0} = \frac{g_m R_C}{2} = -\frac{A_{dd}}{2}$$

Differential-Mode Input Resistance

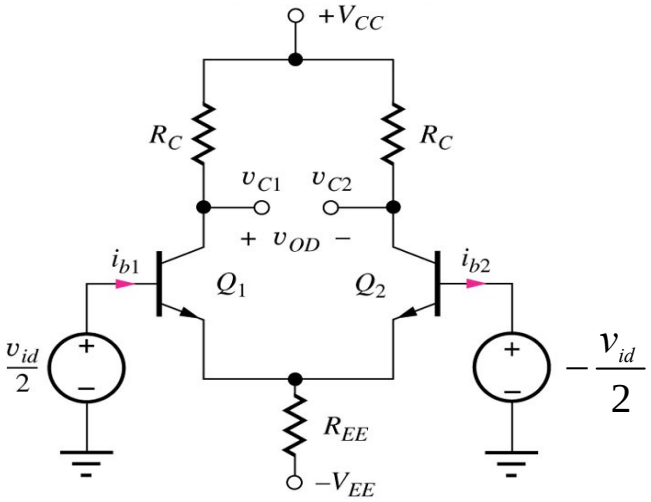


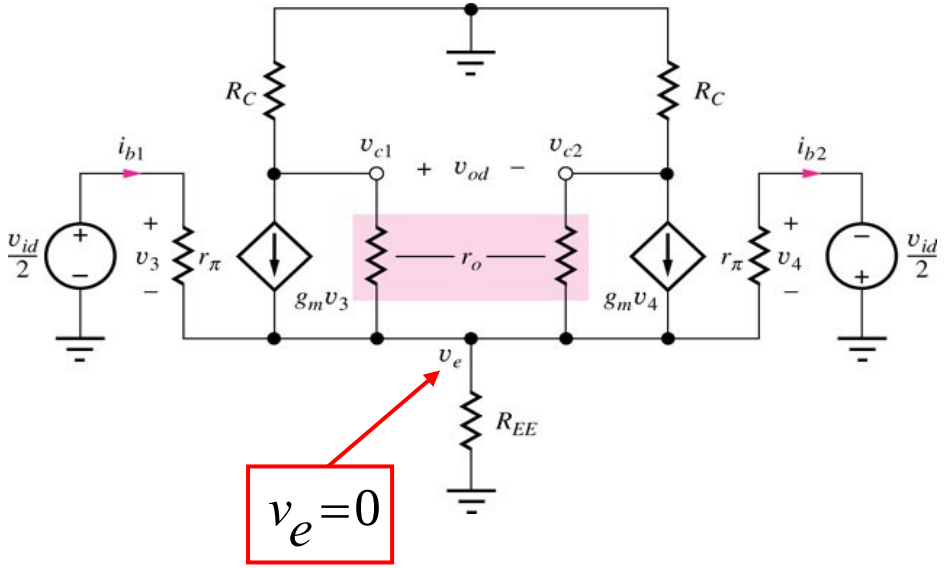


Differential-mode input resistance:

$$\therefore R_{id} \equiv \frac{v_{id}}{i_{b1}} = 2r_\pi \qquad \text{since} \qquad i_{b1} = \frac{(v_{id}/2)}{r_\pi}$$

Output Resistances





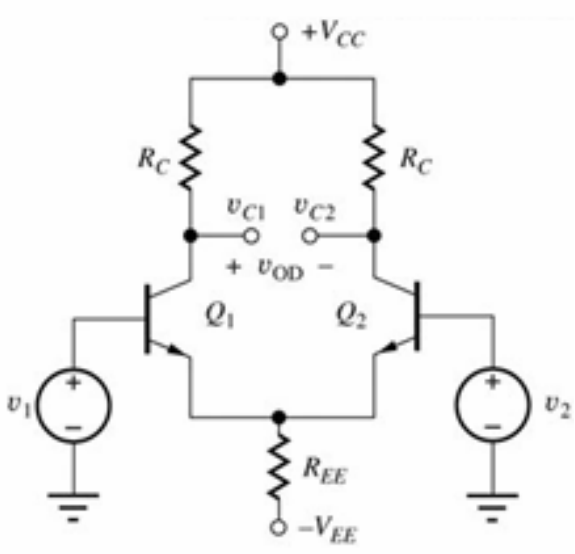
Differential-mode output resistance is the resistance seen between V_{C1} and V_{C2}:

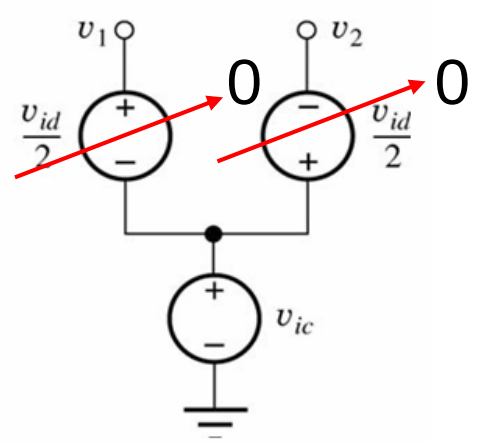
$$R_{od} = 2(R_C \| r_o) \cong 2R_C$$

Single-ended output resistance is the resistance seen between V_{C1} (or V_{C2}) and ground:

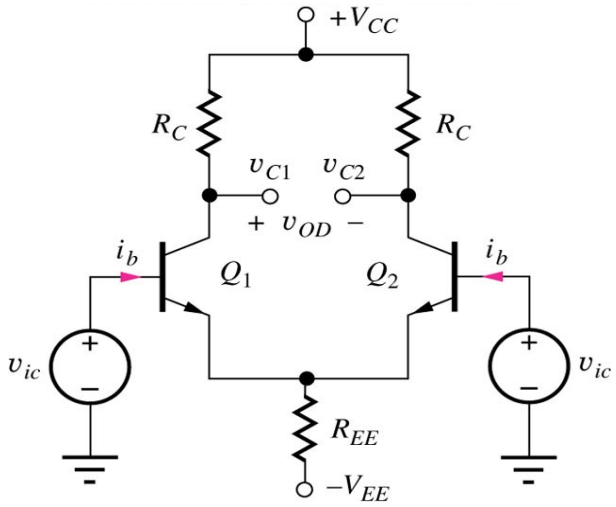
$$R_{od} \cong R_C$$

Common Mode Input

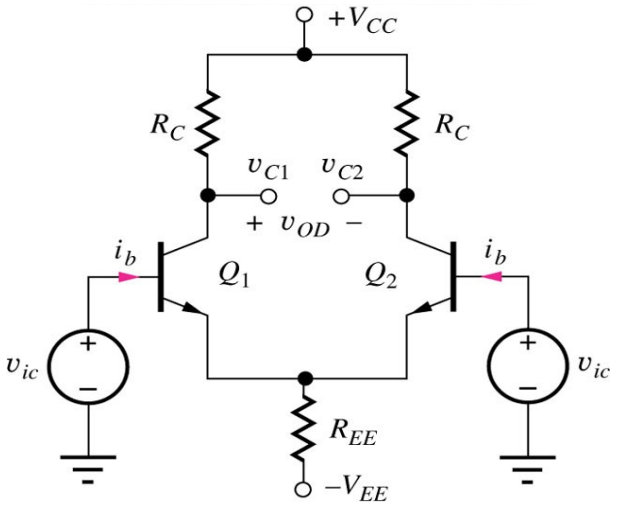


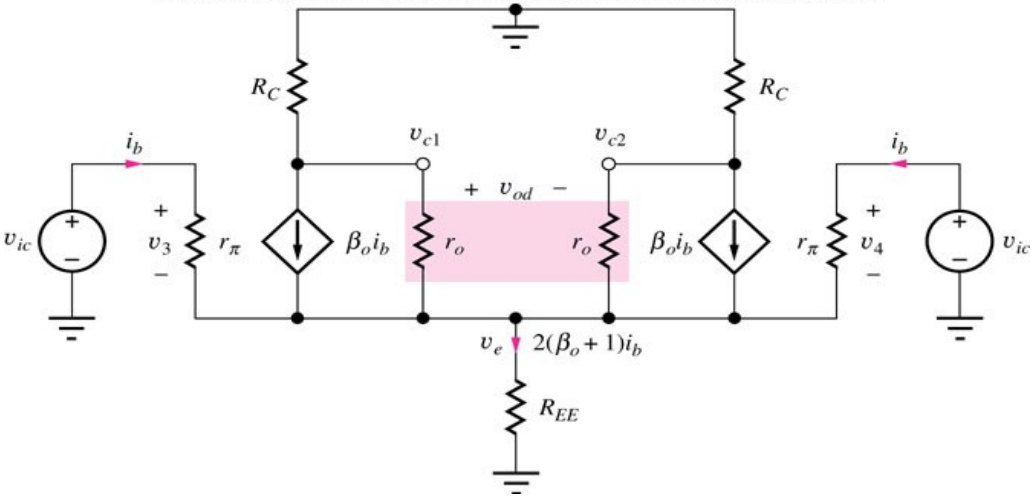


Set differential-mode input to 0:



AC Analysis for Common-Mode Input





Circuit is symmetrical

Ignoring r_o:

$$2(1+\beta)i_b = \frac{v_e}{R_{EE}} \quad \Rightarrow \quad i_b = \frac{v_{ic}}{r_\pi + 2(\beta+1)R_{EE}}$$

$$v_e = v_{ic} - i_b r_\pi$$

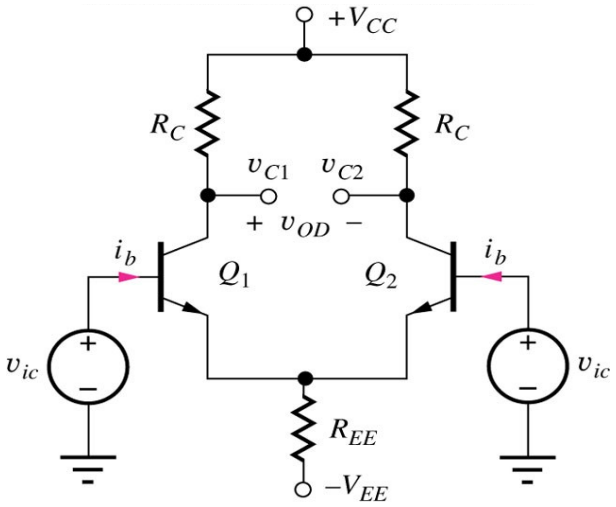
Output voltages are:

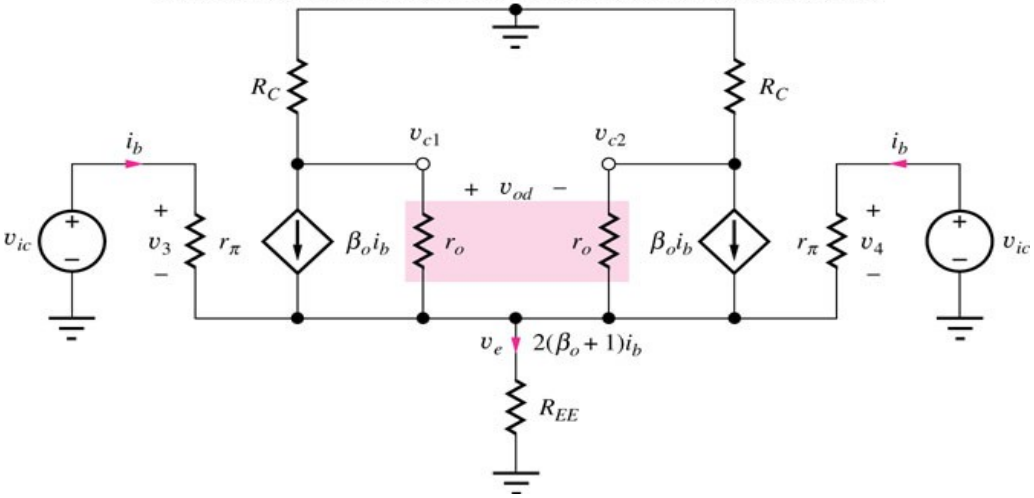
$$v_{c1} = v_{c2} = -\beta i_b R_C = \frac{-\beta R_C}{r_\pi + 2(\beta+1)R_{EE}} v_{ic} \cong \frac{R_C}{2R_{EE}} v_{ic}$$

Differential output = 0

Common-mode voltage gain for single-ended output

Emitter Voltage



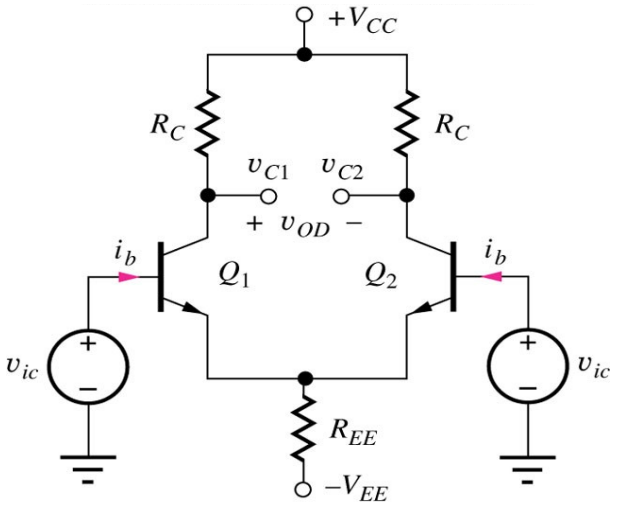


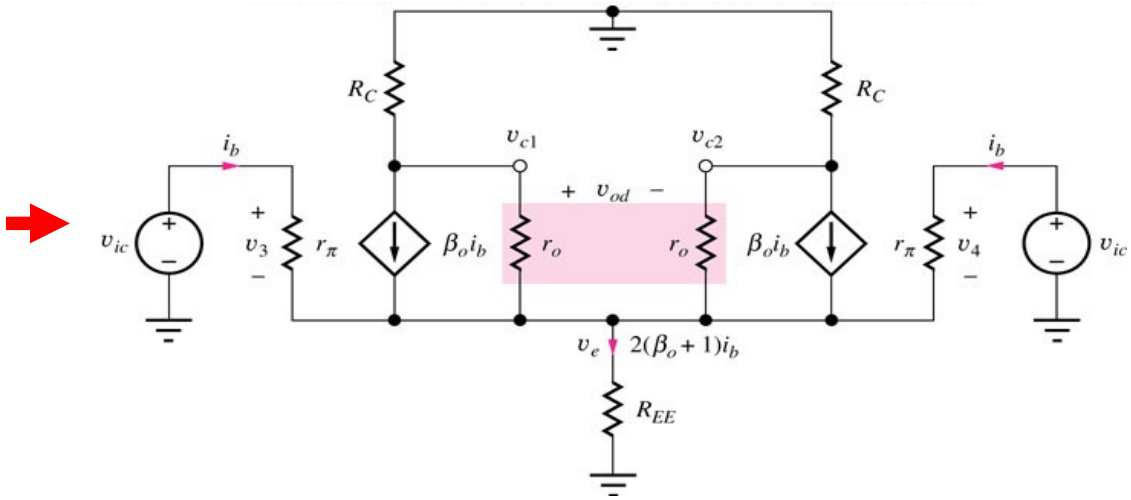
Circuit is symmetrical

$$i_b = \frac{v_{ic}}{r_\pi + 2(\beta+1)R_{EE}} \quad \rightarrow \quad v_e = 2(\beta+1)i_b R_{EE} = \frac{2(\beta+1)R_{EE}}{r_\pi + 2(\beta+1)R_{EE}} v_{ic} \cong v_{ic}$$

Emitter not AC ground for CM input.

Common-Mode Input Resistance





Circuit is symmetrical

CM input resistance is the resistance seen between the shorted bases (V_{ic}) and ground:

$$R_{ic} = \frac{v_{ic}}{2i_b} = \frac{r_\pi + 2(\beta+1)R_{EE}}{2} = \frac{r_\pi}{2} + (\beta+1)R_{EE}$$

Two i_b are drawn from the input voltage source consisting two parallel V_{ic}.

Common-Mode Rejection Ratio

- CMRR is defined as

$$\text{CMRR} \equiv \left| \frac{A_{dm}}{A_{cm}} \right|$$

  – represents ability of amplifier to amplify desired DM input signal and reject undesired CM input signal.

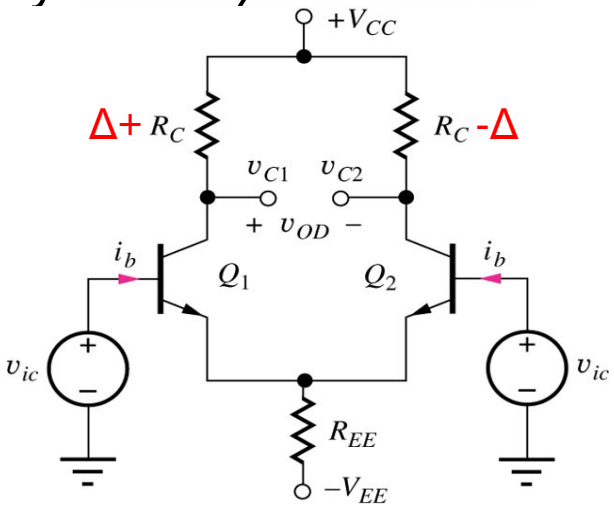
- For output defined differentially, the common-mode gain of a balanced amplifier is zero → CMRR is infinite
  – Many noises appear in common form to the input and thus do not appear at the output

Resistor Mismatch

- Consider mismatches between R_C (which always exists):

$$v_{c1} \cong -\frac{R_{C1}}{2R_{EE}} v_{ic} \qquad v_{c2} \cong -\frac{R_{C2}}{2R_{EE}} v_{ic}$$

$$v_{od} = v_{c1} - v_{c2} \cong \frac{R_{C2} - R_{C1}}{2R_{EE}} v_{ic} = \frac{\Delta R_C}{R_C} \frac{R_C}{2R_{EE}} v_{ic}$$



where $\frac{\Delta R_C}{R_C} = \frac{R_{C1} - R_{C2}}{(R_{C1} + R_{C2})/2}$ represents fractional mismatch

$$\therefore \text{CMRR} \equiv \left|\frac{A_{dm}}{A_{cm}}\right| = \frac{g_m R_C}{\frac{\Delta R_C}{R_C}\frac{R_C}{2R_{EE}}} = g_m R_{EE} \left(\frac{\Delta R_C}{R_C}\right)^{-1}$$

➡ R_{EE} should be maximized for good CMRR

DM and CM Gains

Define the DM and CM outputs as

$$v_{od} = v_{c1} - v_{c2}$$

$$v_{oc} = \frac{v_{c1} + v_{c2}}{2}$$

Output and input are related by the gain matrix:

$$\begin{bmatrix} v_{od} \\ v_{oc} \end{bmatrix} = \begin{bmatrix} A_{dd} & A_{cd} \\ A_{dc} & A_{cc} \end{bmatrix} \begin{bmatrix} v_{id} \\ v_{ic} \end{bmatrix}$$

where

A_{dd} = differential-mode gain

A_{cd} = common-mode to differential-mode conversion gain

A_{cc} = common-mode gain

A_{dc} = differential mode to common-mode conversion gain

For ideal symmetrical amplifier,

$A_{cd} = A_{dc} = 0$.

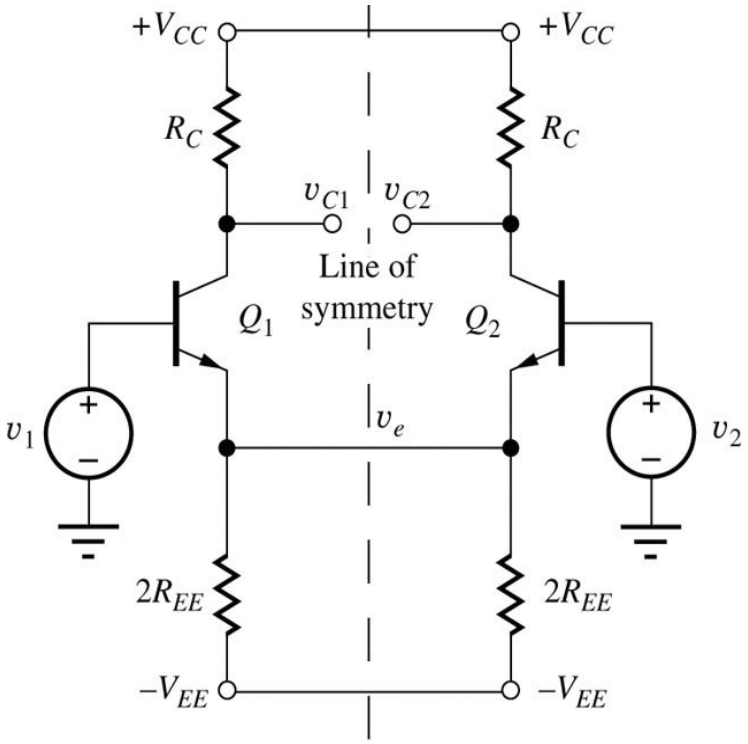
$$\therefore \begin{bmatrix} v_{od} \\ v_{oc} \end{bmatrix} = \begin{bmatrix} A_{dd} & 0 \\ 0 & A_{cc} \end{bmatrix} \begin{bmatrix} v_{id} \\ v_{ic} \end{bmatrix}$$

Purely differential-mode input gives purely differential-mode output and vice versa.

Topics to cover …

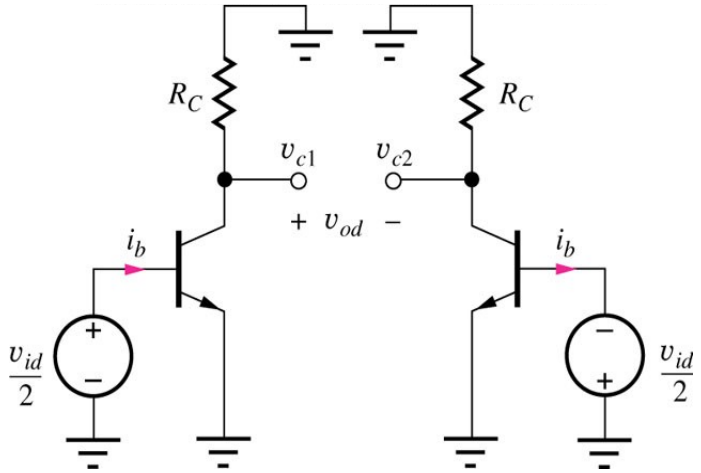
- Large signal analysis
- AC analysis
- Half-circuit analysis

Half-Circuit Analysis



- Redraw the differential amplifier in a fully symmetrical form
  - power supplies are split into two equal halves in parallel
  - emitter resistor is separated into two equal resistors in parallel
- For differential mode signals, points on the line of symmetry are grounds for ac analysis
  - V_{CC} and V_{EE} are AC grounds
  - v_e is AC ground as proven previously
- For common-mode signals, points on line of symmetry are replaced by open circuits
  - b/c no current flows across the line of symmetry

Differential-mode Half-circuits



- The two power supply lines and emitter become ac grounds
- The half-circuit represents a C-E amplifier stage

Direct analysis of the half-circuits yield:

$$v_{c1} = -g_m R_C \frac{v_{id}}{2}$$

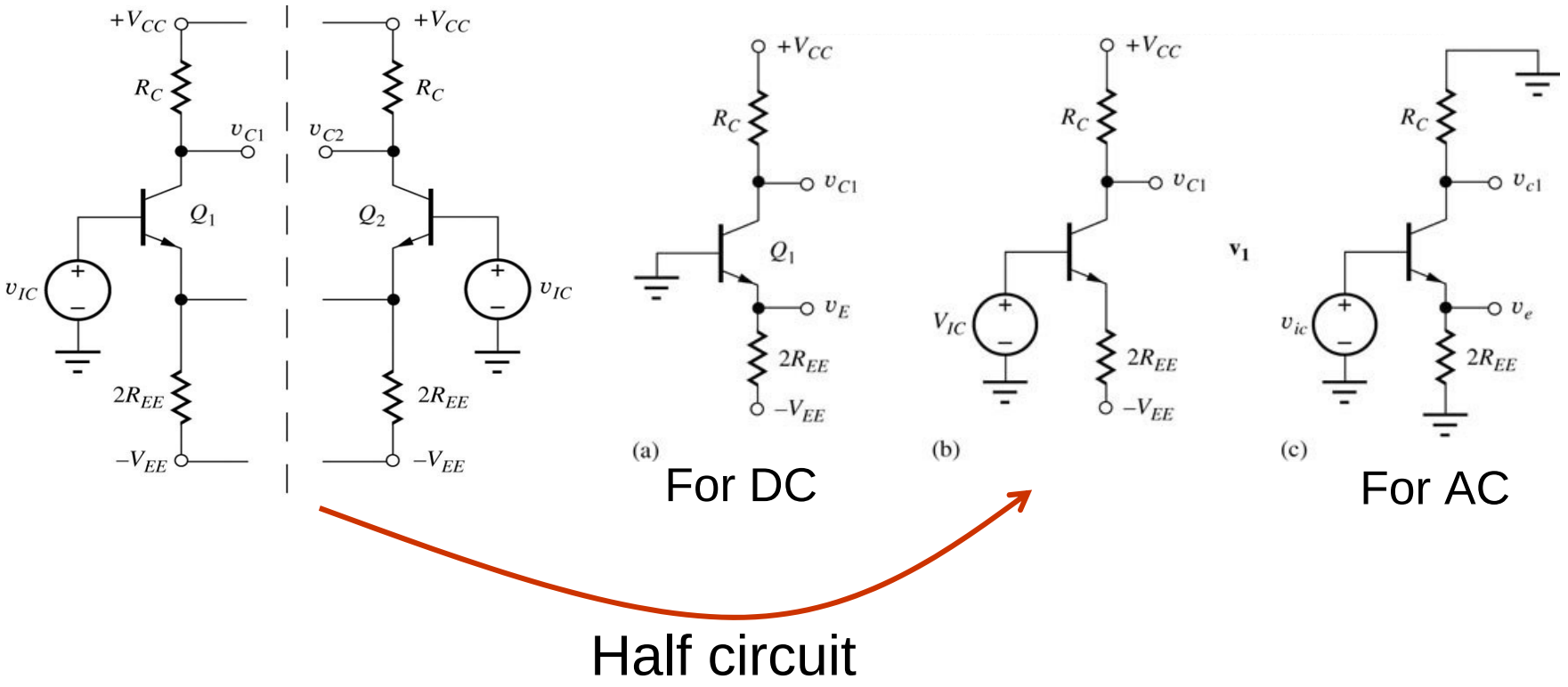
$$v_{c2} = +g_m R_C \frac{v_{id}}{2}$$

$$v_o = v_{c1} - v_{c2} = -g_m R_C v_{id}$$

$$R_{id} = v_{id} / i_{b1} = 2r_\pi$$

$$R_{od} = 2(R_C \| r_o)$$

Common-mode Half-circuit



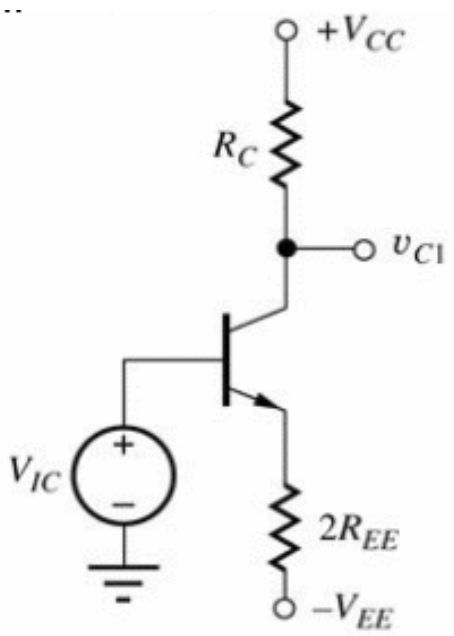
- All points on line of symmetry become open circuits

Common-mode Input Voltage Range

- The CM input signal range for small-signal assumption to be valid is similar to that of an emitter-degenerated CE amplifier:

$$v_{ic} \leq 5mV(1+g_m 2R_{EE})$$

- R_{EE} is very large in most cases
  → Wide common-mode input range



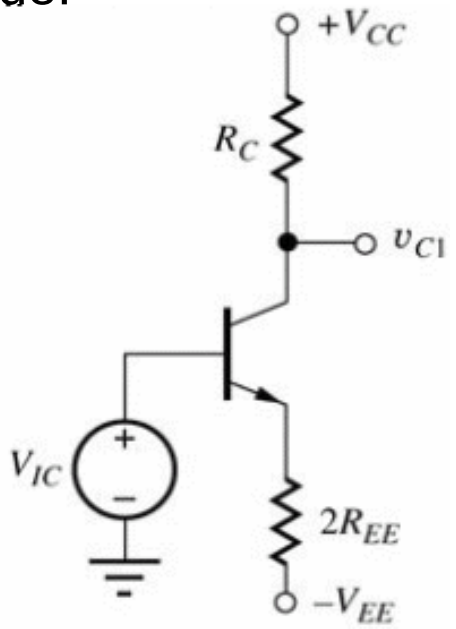
CM Input Voltage Range

Another condition is that BJT must be in active mode:

$$V_{CB} = V_{CC} - I_C R_C - V_{IC} \geq 0$$

$$I_C = \alpha \frac{V_{IC} - V_{BE} + V_{EE}}{2R_{EE}}$$

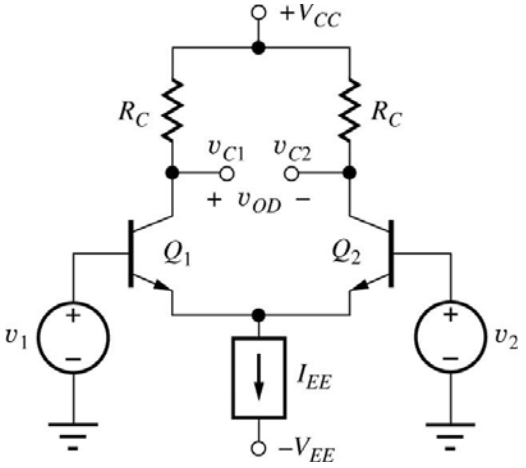
$$\therefore V_{IC} \leq \frac{V_{CC} - \dfrac{\alpha R_C \left(V_{EE} - V_{BE} \right)}{2R_{EE}}}{1 + \dfrac{\alpha R_C}{2R_{EE}}}$$

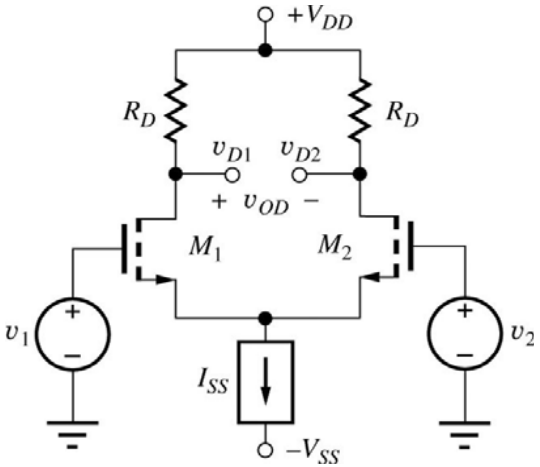


For example, if $V_{CC}=V_{EE}$, $V_{EE} >> V_{BE}$, and $R_C = R_{EE}$,

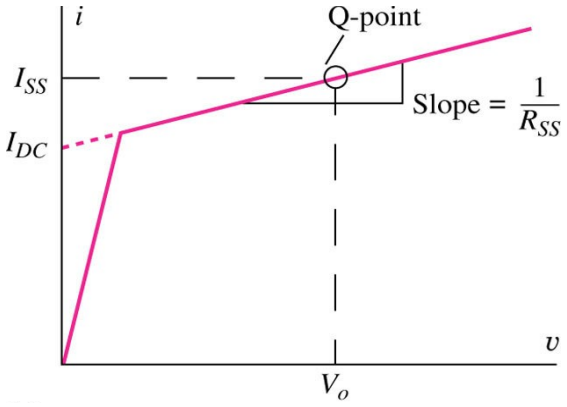
$$V_{IC} \leq \frac{V_{CC}}{3}$$

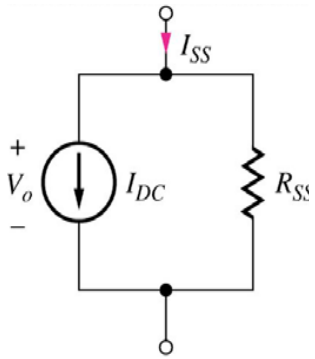
Biasing with Current Source





- Differential amplifiers biased using current sources has
  - A more stabilized operating point
  - A higher effective value of R_{EE} to improve CMRR

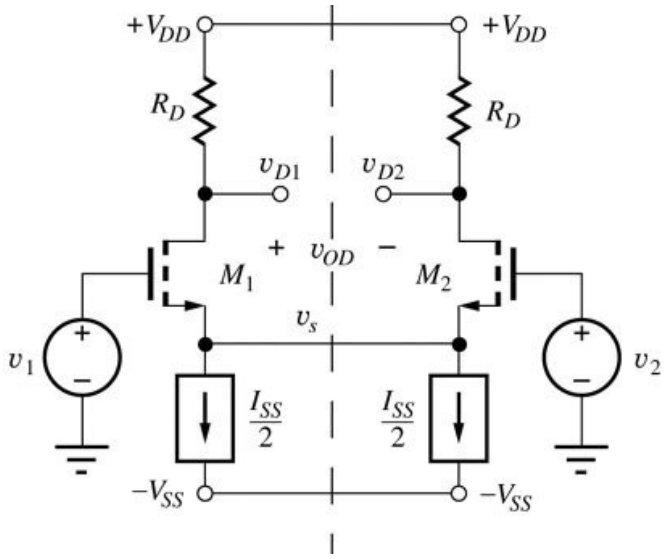


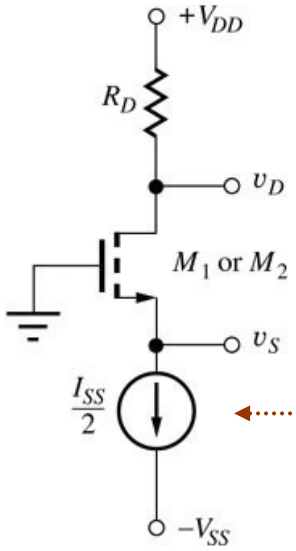


Equivalent of I_{ss}

$$I_{DC} = I_{SS} - \frac{V_0}{R_{SS}}$$

DC Analysis





$I_S = I_{SS}/2$.

DC Half-circuit

$$I_D = \frac{K_n}{2}\left(V_{GS} - V_{TN}\right)^2$$

$$V_{GS} = V_{TN} + \sqrt{\frac{2I_D}{K_n}} = V_{TN} + \sqrt{\frac{I_{SS}}{K_n}}$$

$$V_{D1} = V_{D2} = V_{DD} - I_D R_D \quad \text{and} \quad V_{OD} = 0$$

$$V_{DS} = V_D - V_S = V_{DD} - I_D R_D + V_{GS}$$

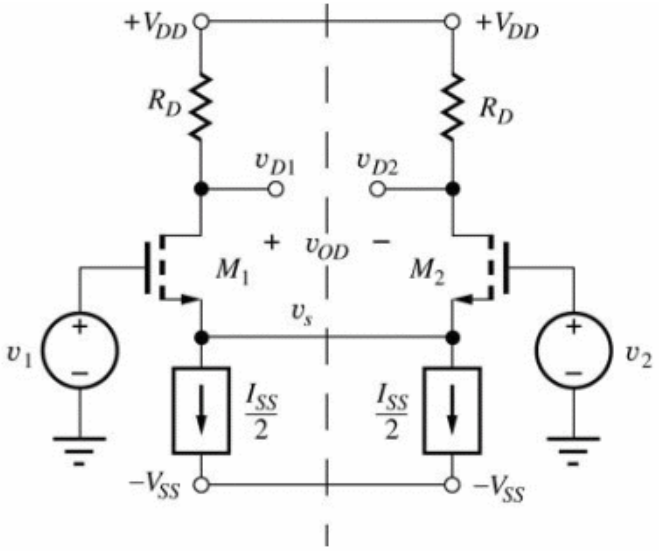
Example

- **Problem:** Find Q-points of transistors in the differential amplifier and the upper limit of input CM voltage.
- **Given data:** V_{DD}=V_{SS}=12 V, I_{SS} =200 μA, R_{SS} = 500 kΩ, R_D = 62 kΩ, λ = 0.0133 V^{-1}, K_n = 5 mA/ V^2, V_{TN} =1V
- **Analysis:**

$$I_D = \frac{I_{SS}}{2} = 100\,\mu\text{A}$$

$$V_{GS} = 1 + \sqrt{\frac{200\,\mu\text{A}}{5\text{mA/V}^2}} = 1.20\text{V}$$

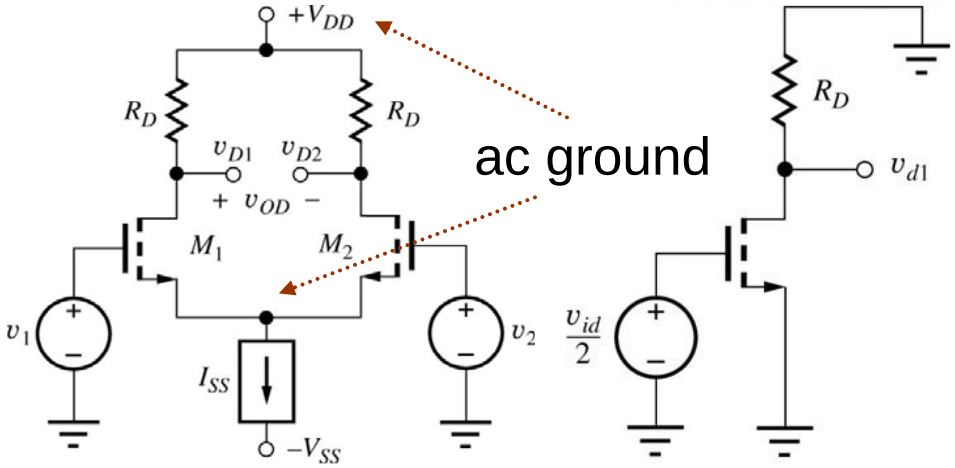
$$V_{DS} = 12\text{V} - (100\,\mu\text{A})(62\text{k}\Omega) + 1.2\text{V} = 7\text{V}$$



To maintain pinch-off operation of M_1 for nonzero V_{IC} ,

$$V_{GD} = V_{IC} - \left(V_{DD} - I_D R_D\right) \le V_{TN}$$
$$\therefore V_{IC} \le V_{DD} - I_D R_D + V_{TN} = 6.8\text{V}$$

Half Circuit for Differential-mode Input



Half Circuit

$$v_{d1} = -g_m R_D \frac{v_{id}}{2}$$

$$v_{d2} = +g_m R_D \frac{v_{id}}{2}$$

$$\therefore v_{od} = -g_m R_D v_{id}$$

Gain for DM output is

$$A_{dd} = \left.\frac{v_{od}}{v_{id}}\right|_{v_{ic}=0} = -g_m R_D$$

Gain for single-ended output is

$$A_{dd1} = \left.\frac{v_{d1}}{v_{id}}\right|_{v_{ic}=0} = -\frac{g_m R_D}{2} = \frac{A_{dd}}{2}$$

$$A_{dd2} = \left.\frac{v_{d2}}{v_{id}}\right|_{v_{ic}=0} = +\frac{g_m R_D}{2} = -\frac{A_{dd}}{2}$$

DM input and output resistance:

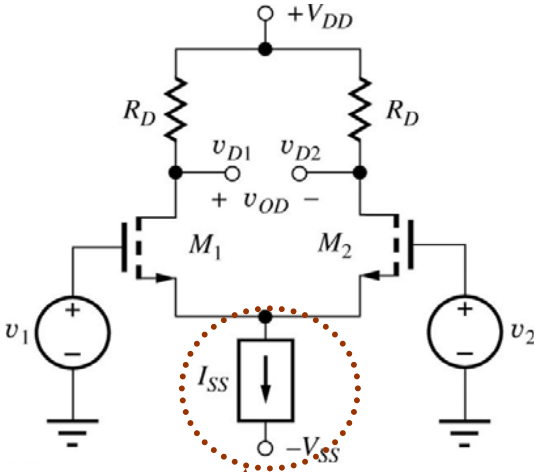
$$R_{id} = \infty \qquad R_{od} = 2R_D$$

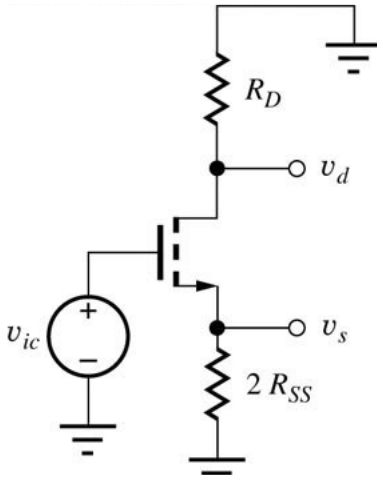
Reference Equations

SINGLE TRANSISTOR FET AMPLIFIERS — APPROXIMATE EXPRESSIONS

	COMMON-SOURCE	COMMON-DRAIN	COMMON-GATE
Terminal voltage gain	$\cong -\frac{g_m R_L}{1 + g_m R_S}$	$\cong +\frac{g_m R_L}{1 + g_m R_L} \cong +1$	$+g_m R_L$
Input resistance	∞	∞	$1/g_m$
Output resistance	$r_o(1 + g_m R_S)$	$1/g_m$	$r_o(1 + g_m R_{th})$
Input signal range	$0.2(V_{GS} - V_{TN})(1 + g_m R_S)$	$0.2(V_{GS} - V_{TN})(1 + g_m R_L)$	$0.2(V_{GS} - V_{TN})(1 + g_m R_{th})$
Current gain	∞	∞	1

Half Circuit for Common-mode Input

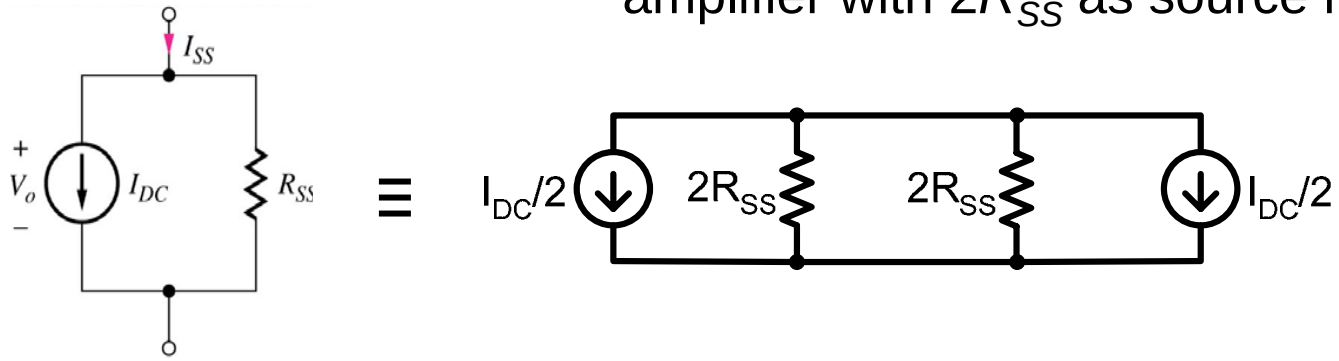




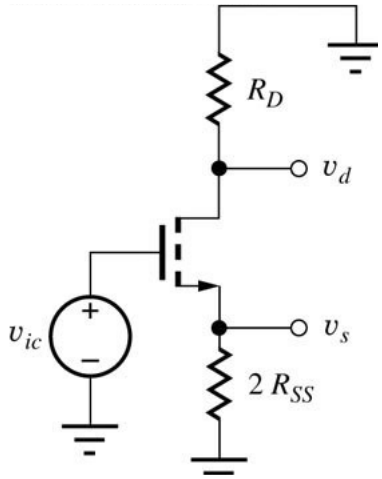
Half Circuit

Rss = Two $2R_{ss}$ in parallel

Common-mode half-circuit = common-source amplifier with $2R_{SS}$ as source resistor



AC Analysis for CM Input



Half Circuit

$$v_{d1} = v_{d2} = \frac{-g_m R_D}{1+2g_m R_{SS}} v_{ic}$$

Common-mode gain:

$$A_{cc} = \left.\frac{v_{oc}}{v_{ic}}\right|_{v_{id}=0} = -\frac{g_m R_D}{1+2g_m R_{SS}} \cong -\frac{R_D}{2R_{SS}}$$

CM input to DM output conversion gain = 0 because

$$v_{od} = v_{d1} - v_{d2} = 0$$

Common-mode input resistance:

$$R_{ic} = \infty$$

Common-Mode Rejection ratio

- For DM output,

$$\text{CMRR} = \left|\frac{A_{dm}}{A_{cm}}\right| = \frac{|A_{dm}|}{0} \to \infty$$

  - Mismatch will result in finite CMRR as in the BJT differential pair.

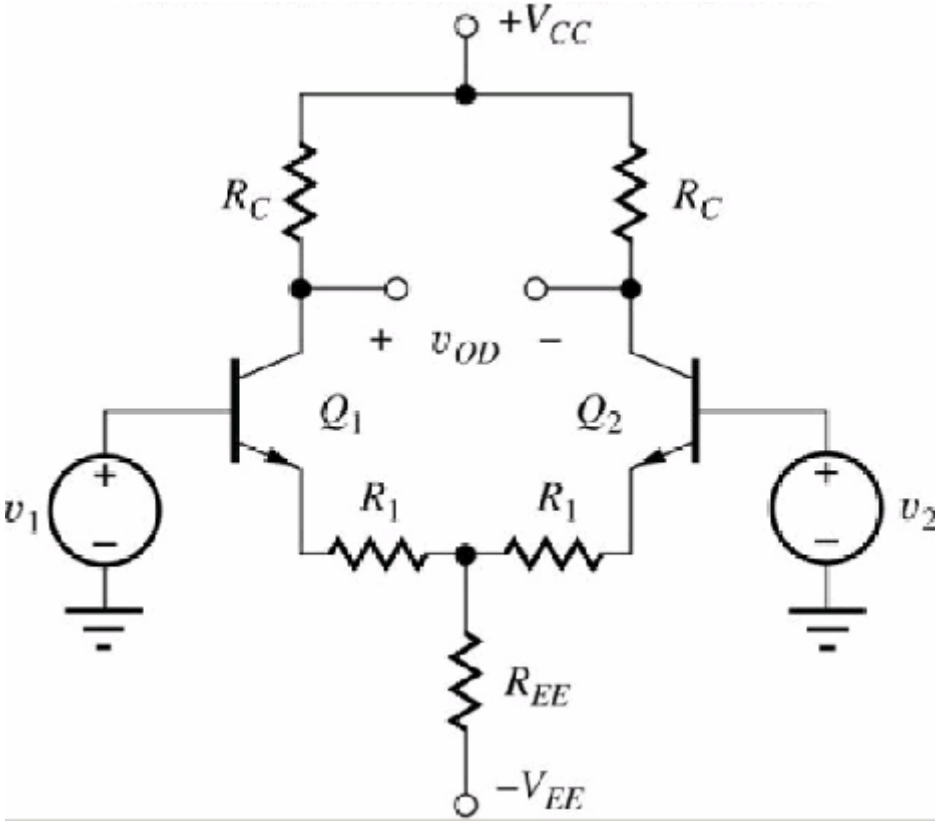
- For single-ended output,

$$\text{CMRR} = \left|\frac{A_{dm}}{A_{cm}}\right| = \left|\frac{A_{dd}/2}{A_{cc}}\right| = \left|\frac{-(g_m R_D)/2}{-R_D/(2R_{SS})}\right| = g_m R_{SS}$$

  - R_{SS} should be maximized

Class Exercise

Draw the common-mode and differential-mode half circuits for the differential pair shown below.



Summary

- Properties of the differential pair
  - It amplifies difference between input voltages and reject their common-mode component
    - Most noises, such as power supply noise, appear to be common mode signal and not amplified by the amplifier.
  - CMRR represents its ability to reject CM input signal.
  - It can produce AC ground (for DM input) at emitter without using bypass capacitors
  - Input common mode range is very wide
- Half circuit analysis technique
  - Points on the line of symmetry are open-circuits for CM signal
  - Points on the line of symmetry are AC grounds for DM signal