ELE 2110A Electronic Circuits

Week 5: BJT Biasing and Small Signal Model



Lecture 05 - 1

Topics to cover ...

- BJT Amplifier Biasing Circuits
- Small Signal Operation and Equivalent Circuits

Reading Assignment: Chap 13.1 – 13.6 of Jaeger and Blalock , or Chap 5.5 - 5.7 of Sedra & Smith



BJT as Amplifier: Example 1

Problem: Determine the dc voltage transfer characteristic of the circuit for 0 < v₁ <5 V
Analysis:

For $v_1 \le 0.7$ V, Q is cut off and $v_0 = 5$ V.

For $v_1 > 0.7$ V, Q turns on and is in the active mode, so that

$$i_{B} = \frac{V_{I} - V_{BE}}{R_{B}} = \frac{V_{I} - 0.7}{100 \text{k}\Omega}$$

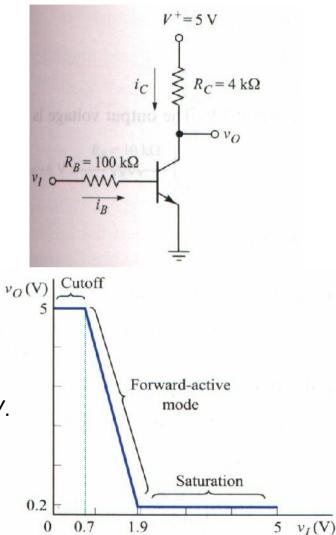
The output voltage is

$$\mathbf{v}_{o} = \mathbf{V}^{+} - \mathbf{i}_{c}\mathbf{R}_{c} = \mathbf{V}^{+} - \beta \mathbf{i}_{B}\mathbf{R}_{c}$$
$$\mathbf{v}_{o} = 5 - (100) \left[\frac{\mathbf{v}_{I} - 0.7}{100 \mathrm{k}\Omega}\right] 4\mathrm{k}\Omega$$

or

This equation is valid for $v_1 \ge 0.7$ V and $v_0 \ge v_{CE}(\text{sat}) = 0.2V$.

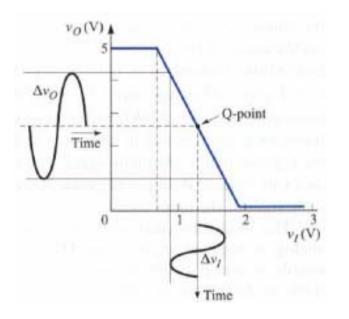
The input voltage for $v_o = 0.2$ V is found to be $v_i = 1.9$ V. Now, for $v_i > 1.9$ V, the transistor is in saturation.

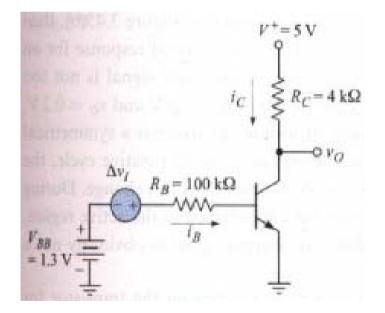




Conceptual Bias Circuit for BJT

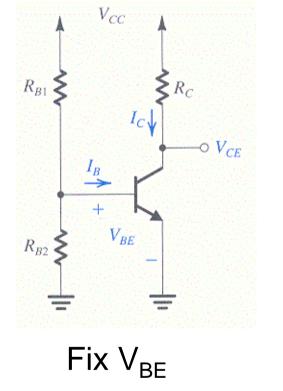
- Keep the transistor in the active mode;
- Establish a Q-point near the center of the active region;
- Couple the time-varying signal to the base.



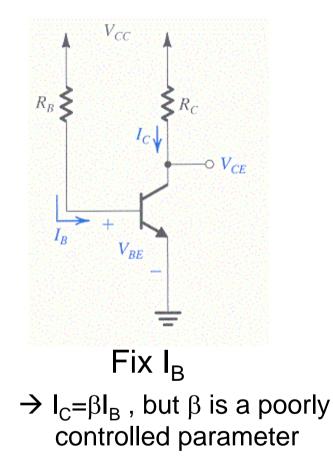




Two Obvious Bias Circuits



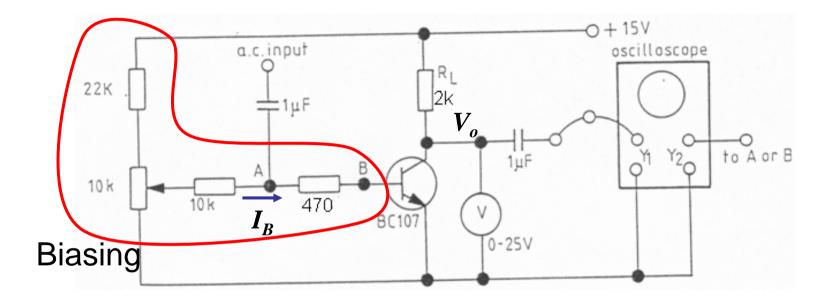
→ I_C is an exponential function of V_{BE} and thus V_{CC}



- \rightarrow Wide variations in $I_{\rm C}$ and hence in $V_{\rm CE}$
- \rightarrow "Bad" biasing schemes



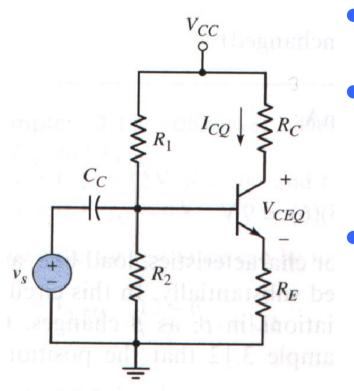
Biasing Circuit in ERG2810 Experiment A3



- Adjusting the variable resistor to give a desired amount of I_B such that V_o is at about 8V (half the supply voltage).
- The transistor operates at the middle of active region.

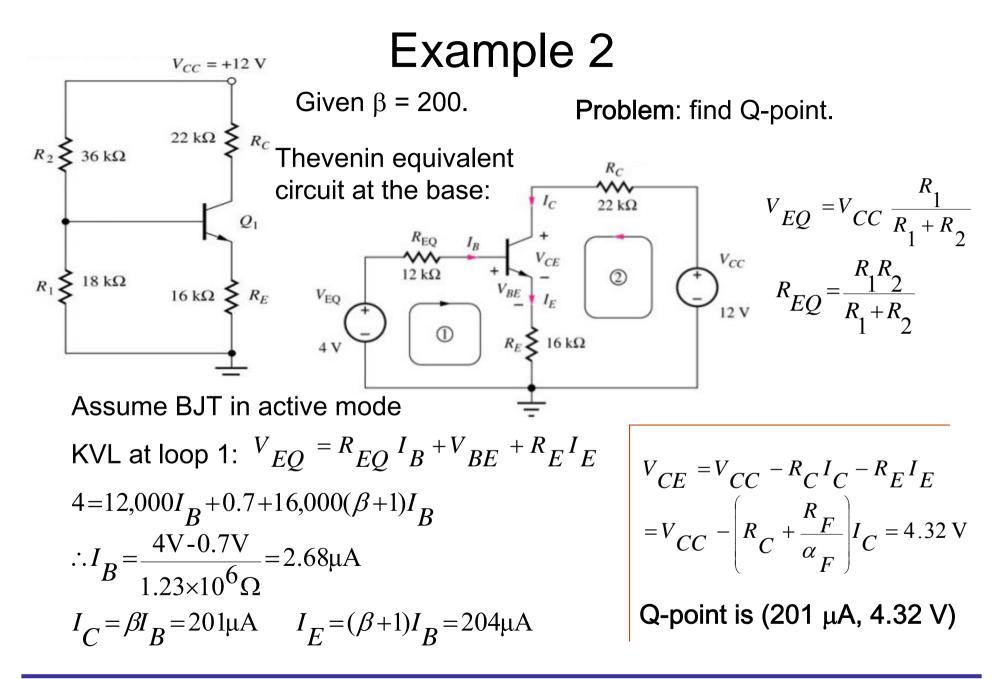


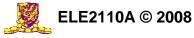
Classical Four-Resistor Bias Circuit



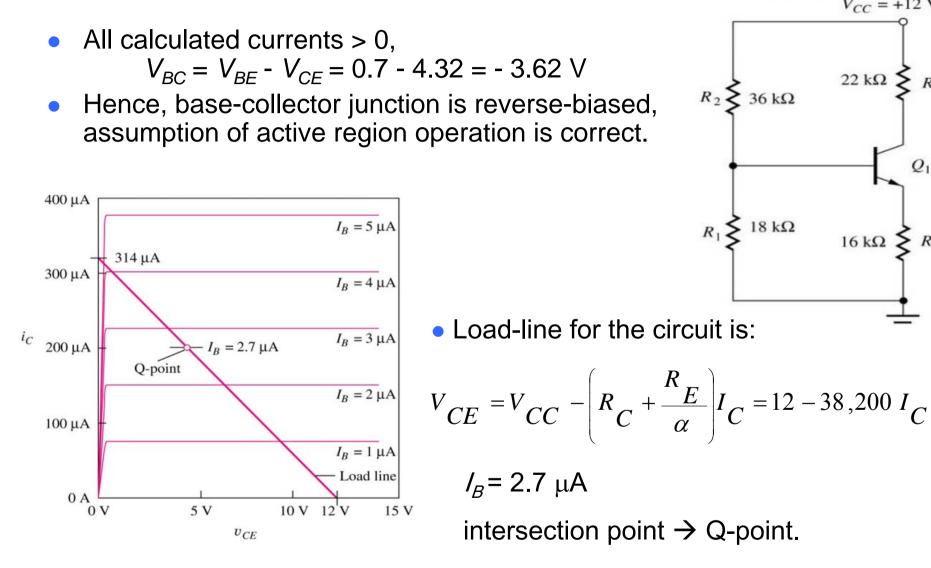
- V_B established by the voltage divider formed by R_1 and R_2 .
- R_E added → reduce sensitivity to supply voltage, process, and temperature variations
 → to be discussed later
- Coupling capacitor C_{c} :
 - open circuit to DC, isolating the signal source from the dc biasing current.
 - short circuit to AC signal (if the signal frequency is large enough and C_C is large enough).
- The Q-point is usually specified by (I_C, V_{CE}) for *npn* transistor or (I_C, V_{EC}) for *pnp* transistor.

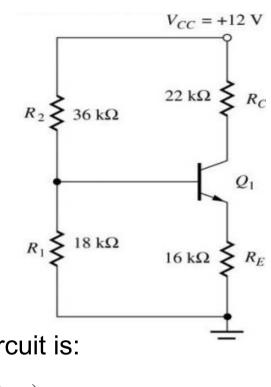






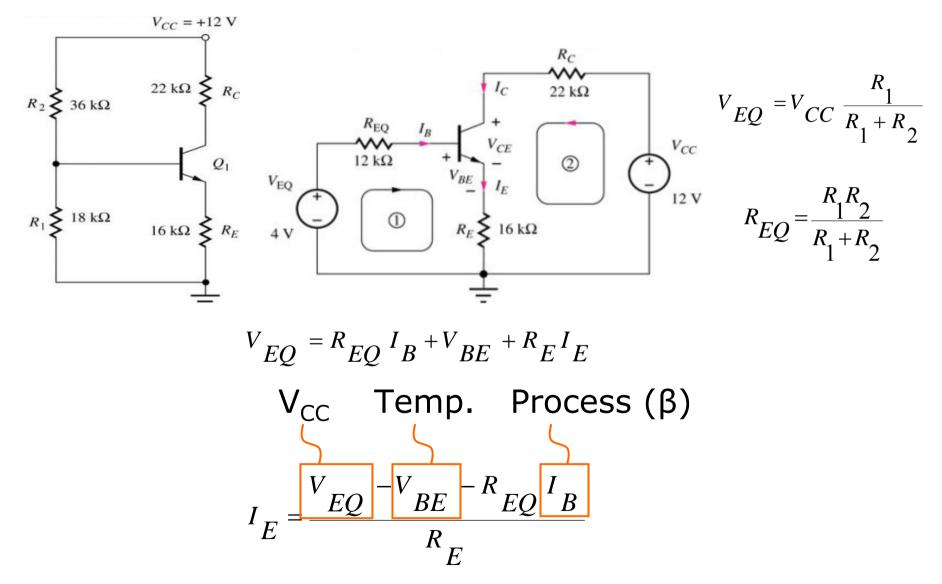
Example 2 (Cont')







Example 2 (Cont')





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Design Objectives: Q-point Insensitive to PVT Variations

$$I_E = \frac{V_{EQ} - V_{BE} - R_{EQ}I_B}{R_E}$$

- 1) I_E linearly (not exponentially) related to V_{CC}
- 2) For I_E to be less sensitive to I_B (thus β):

$$\rightarrow R_{EQ} I_B \ll (V_{EQ} - V_{BE})$$

- \rightarrow Need small R_{eq}
- \rightarrow Large currents through R₁ and R₂ (I₂ >> I_B)
- For I_E to be less sensitive to V_{BE} (due to temperature change):
 → V_{EQ} >> V_{BE}

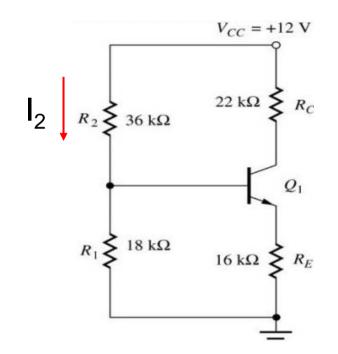


Design Objectives: Low Power and Large Signal Swing

But ...

- For low power consumption:
 - \rightarrow needs small I₂
 - \rightarrow contradict with constraint (2)
 - \rightarrow set I₂ = 10I_B typically
- For large output signal swing:
 → V_{EQ} cannot be too high (because V_C∈ [V_{EQ}, V_{CC}])

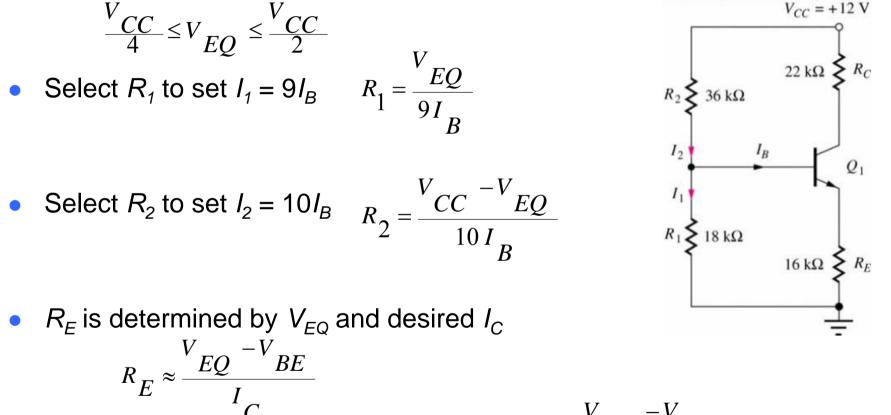
$$\rightarrow$$
 V_{EQ} =1/3 V_{CC} typically



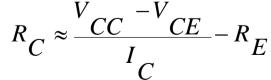


Design Guidelines

Choose Thevenin equivalent base voltage







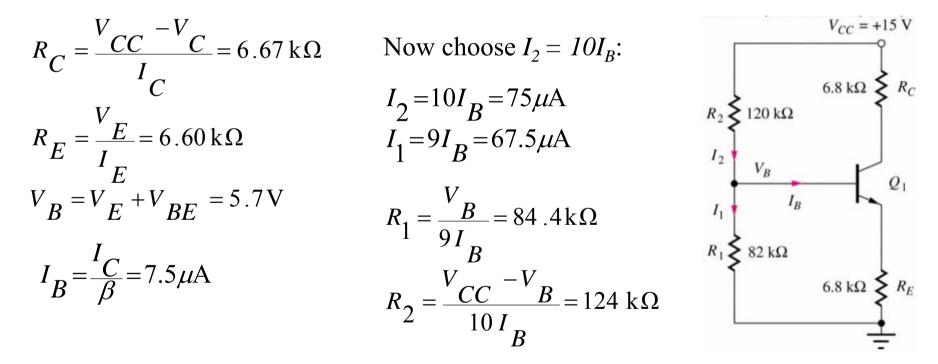


 $V_{CC} = +12 \text{ V}$

 $^{22 k\Omega} \begin{cases} R_C \end{cases}$

Example 3

- **Problem:** Design a 4-resistor bias circuit with given parameters.
- Given data: $I_C = 750 \ \mu\text{A}, V_{CE} = 5 \ \text{V}, \beta = 100, V_{CC} = 15 \ \text{V}, V_{BE} = 0.7 \ \text{V}$
- Unknowns: V_B , voltages across R_E and R_C ; values for R_1 , R_2 , R_C and R_E .
- Analysis: A common approach is to divide $(V_{CC} V_{CE})$ equally between R_E and R_C . Thus, $V_E = 5$ V and $V_C = 10$ V.





Example 4: Two-Resistor Bias Network

- **Problem:** Find Q-point for *pnp* transistor in 2-resistor bias circuit with given parameters.
- Given data: $\beta_F = 50$, $V_{CC} = 9$ V

 V_{EB}

 $18 k\Omega$

 $1 k\Omega$

- Assumptions: Forward-active operation region, $V_{EB} = 0.7 \text{ V}$
- Analysis:

 V_{EC}

 I_C

$$9 = V_{EB} + 18,000 I_{B} + 1000 (I_{C} + I_{B})$$

$$\therefore 9 = V_{EB} + 18,000 I_{B} + 1000 (51)I_{B}$$

$$\therefore I_{B} = \frac{9V - 0.7V}{69,000 \Omega} = 120 \mu A$$

$$I_{C} = 50 I_{B} = 6.01 \, \text{mA}$$

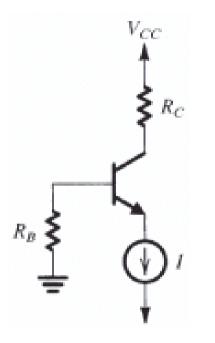
$$V_{EC} = 9 - 1000 (I_{C} + I_{B}) = 2.88 \, \text{V}$$

$$V_{BC} = 2.18 \, \text{V}$$

Q-point is : (6.01 mA, 2.88 V)



Current Source Biasing

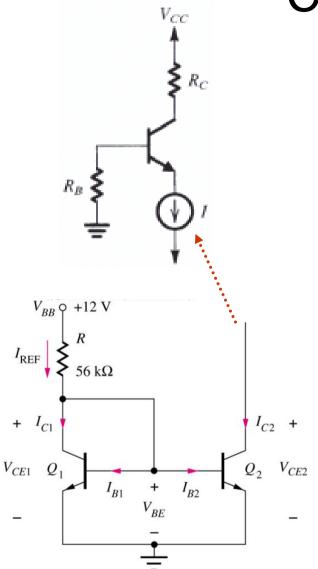


• $I_E = I \rightarrow$ independent of the value of β and temperature



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Current Source Implementation: Current Mirror



- Use collector current of a transistor in active mode
- Neglect Early effect, I_{C2} is independent of V_{CE2} as long as $V_{CE2} > V_{CEsat}$ (i.e. BJT in active mode)
- For matched Q_1 and Q_2 , i.e., having identical I_S , β , V_A), we have

$$I_{C2} = I_{REF}$$

$$I_{REF} = \frac{V_{BB} - V_{BE}}{R}$$



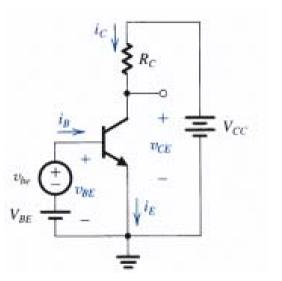
Topics to cover ...

- BJT Amplifier Biasing Circuits
- Small Signal Operation and Equivalent Circuits



BJT as an Amplifier

Conceptual Amplifier circuit:



Superposition of DC with AC signal

If an ac+dc input signal the total v_{BE} becomes

$$v_{BE} = V_{BE} + v_{be}$$

The collector current becomes

$$i_{C} = I_{S} e^{(V_{BE} + v_{be})/V_{T}}$$

= $I_{S} e^{V_{BE}/V_{T}} e^{v_{be}/V_{T}} = I_{C} e^{v_{be}/V_{T}}$



Small-signal Transconductance

 I_C

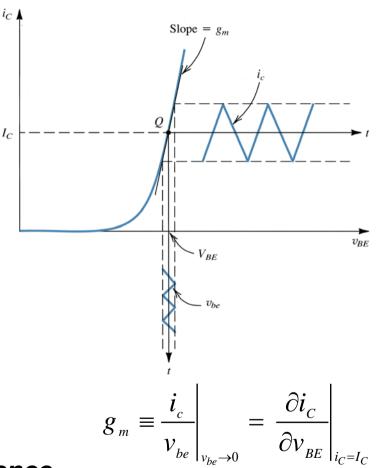
For small ac signal, i.e., $v_{be} \ll V_T$: $i_{C} = I_{C} e^{v_{be}/V_{T}} \cong I_{C} (1 + v_{be}/V_{T})$ $= \underbrace{I_{C}}_{DC} + \underbrace{I_{C}}_{V_{T}} v_{be}$

The ac (or signal) component of the collector current is:

$$i_c = \frac{I_C}{V_T} v_{be}$$

We define: $g_m \equiv \frac{i_c}{v_{be}} = \frac{I_C}{V_T}$

g_m is called the small signal *transconductance*. It represents the slope of $i_{\rm C}$ -v_{BF} curve at the Qpoint.



Signal Component of Base Current

Total base current: i_B

$$=\frac{i_{C}}{\beta}=\frac{I_{C}}{\underbrace{\beta}}+\frac{1}{\underbrace{\beta}}\frac{I_{C}}{V_{T}}v_{be}}{\underbrace{\beta}_{AC}}$$

Signal component of base current:

$$i_{b} = \frac{1}{\beta} \frac{I_{C}}{V_{T}} v_{be} = \frac{g_{m}}{\beta} v_{be}$$

Define:
$$r_{\pi} \equiv \frac{V_{be}}{I_b} = \frac{\beta}{g_m} \text{ or } r_{\pi} = \frac{V_{T}}{I_B}$$

 r_{π} is the small-signal input resistance between base and emitter, looking into the base.



Signal Component of Emitter Current

The total emitter current i_{E:}

$$i_E = \frac{i_C}{\alpha} = \frac{I_C}{\underbrace{\alpha}_{DC}} + \underbrace{\frac{1}{\alpha} \frac{I_C}{V_T} v_{be}}_{AC}$$

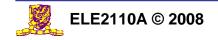
Signal component of emitter current:

$$i_e = \frac{1}{\alpha} \frac{I_C}{V_T} v_{be} = \frac{I_E}{V_T} v_{be}$$

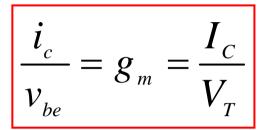
Define:
$$r_e \equiv \frac{v_{be}}{i_e} = \frac{\alpha}{g_m}$$
 or $r_e = \frac{V_T}{I_E}$

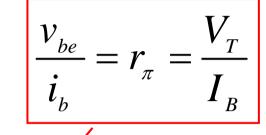
r_e is the small-signal input resistance between base and emitter, *looking into the emitter*.

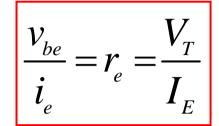
It is easy to find out that $r_{\pi} = (i_e / i_b)r_e = (\beta + 1)r_e$



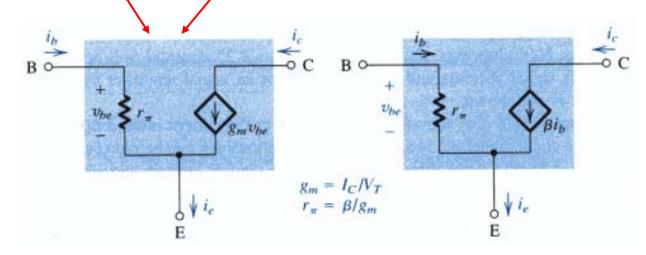
Small Signal I-V Expressions







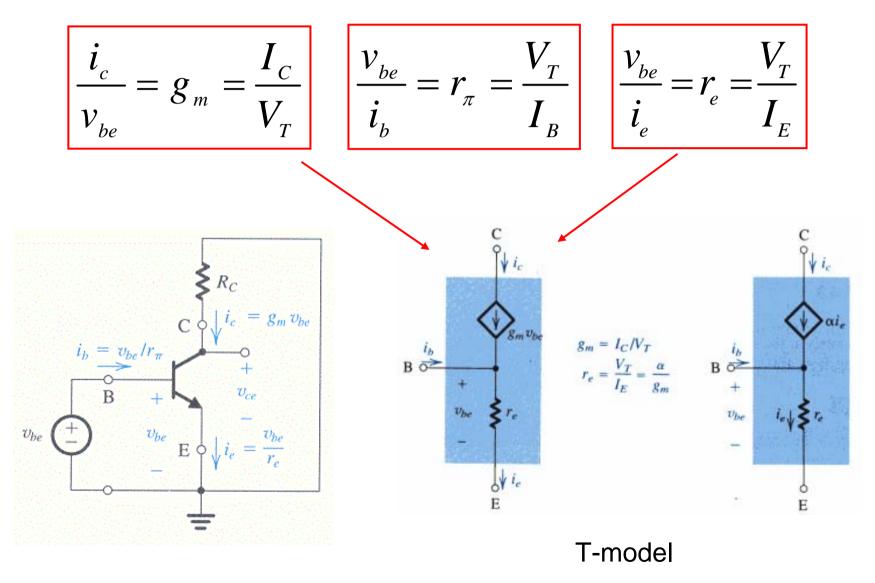
Can be modeled by equivalent circuits:



(*Hybrid-* π small signal model of BJT)

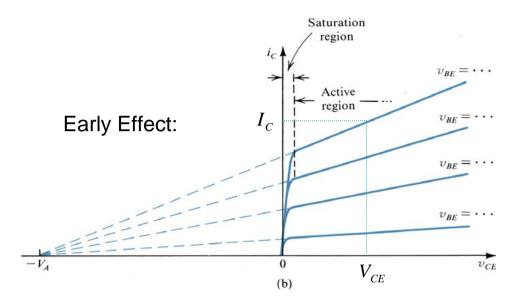


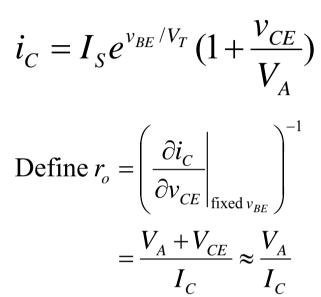
Another model: T-model



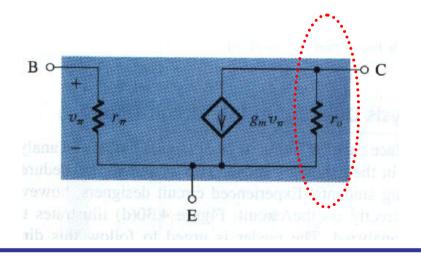


Hybrid- π model including Early effect

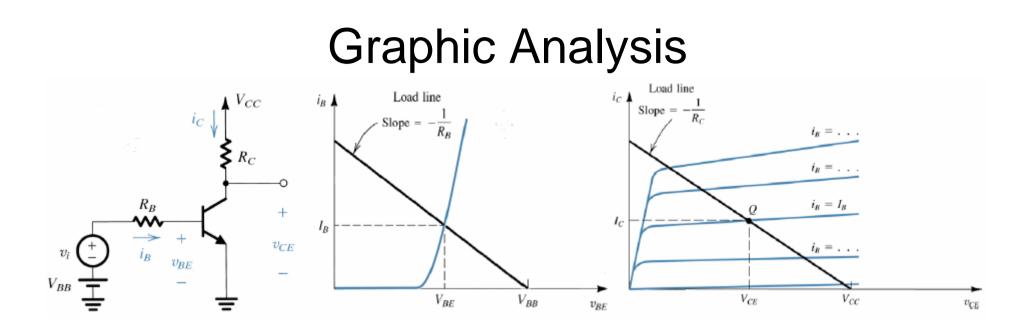




Include Early Effect in the model:





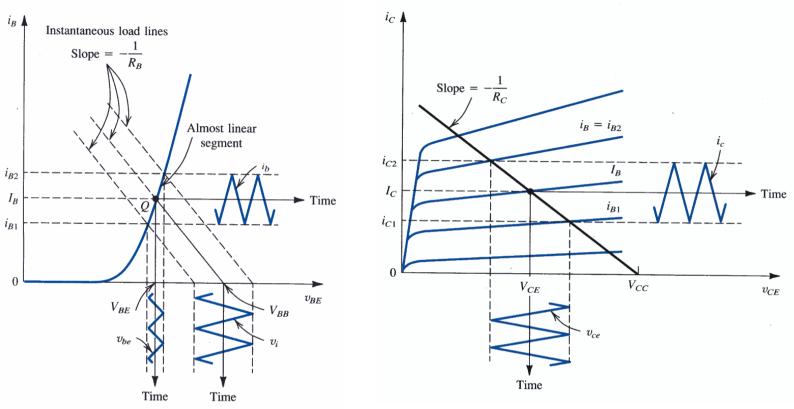


- Can be useful to understand the operation of BJT circuits
- First, establish DC conditions by finding I_B (or V_{BE})
 - Input load line: $v_{BE} = V_{BB} R_B i_B$
- Second, figure out the DC operating point for I_C
 - Output load line:

$$v_{CE} = V_{CC} - i_C R_C \implies i_C = \frac{V_{CC}}{R_C} - \frac{1}{R_C} v_{CE}$$



Graphic Analysis (Cont.)



- Apply a small signal input voltage and see *i_b*
- See how *i_b* translates into *V_{CE}*
- Can get a feel for whether the BJT will stay in active region of operation
 - What happens if R_c is larger or smaller?

