ON AN INDUCTORLESS FM STEREO MULTIPLEX CIRCUIT USING A PHASE-LOCKED LOOP

William J. Padgett
Manager, Product Research
Warwick Electronics, Inc.

Jeffrey N. Denenberg
Senior Engineer
Warwick Electronics, Inc.

INTRODUCTION

Although it was claimed that linear integrated circuits provided cost savings and improved reliability, the introduction of these circuits to consumer applications requiring selectivity was not immediate. In reviewing the IC's, it became obvious that the cost of selectivity negated some of the advantages that were gained by their use.

Therefore, a program was initiated to investigate the feasibility of eliminating coils while obtaining the desired selectivity characteristics through circuit techniques applicable to micro-circuit technology. The results of the investigation are presented by describing an experimental FM stereo multiplex demodulator circuit designed for integration. The system block diagram and circuitry are described and the test results are compared with standard production circuits.

The system block diagram for the FM stereo multiplex demodulator is shown in Figure 1. The stereo composite input signal consists of left plus right audio, left minus right double sideband suppressed carrier modulated on a 38kHz subcarrier, and a 19kHz pilot signal modulated approximately 10%. SCA modulation may also be present.

The selectivity required to recover the 19kHz pilot approximately 20 db down in the "noise" is obtained from a phase locked loop. The 38kHz re-inserted carrier is also generated within the loop and is fed to a synchronous detector for demodulation of the left and right audio channels.

THE PHASE LOCKED LOOP

Detailed mathematical analyses of the basic phase locked loop (PLL) are described in the literature[1]. A review of the PLL follows (see Figure II).

A phase detector can be defined as any circuit which gives an output voltage approximately proportional to the phase difference between two periodic input waveforms of the same frequency. In the PLL stereo demodulator, one of the input waveforms is the 19kHz pilot. The other waveform is the output of a voltage controlled oscillator (VCO).

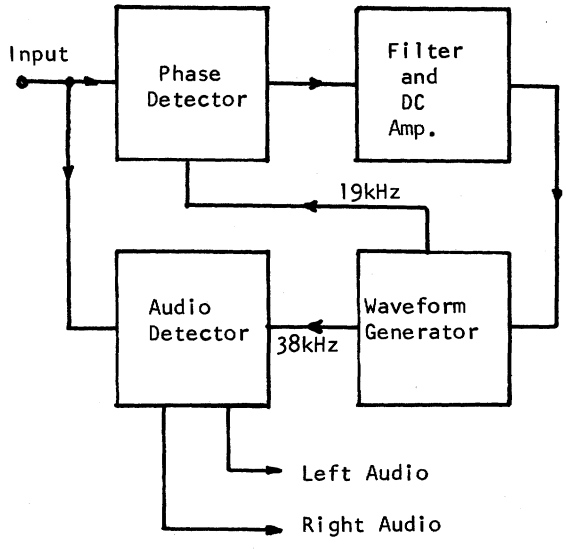

Fig. 1 Stereo Multiplex Demodulator

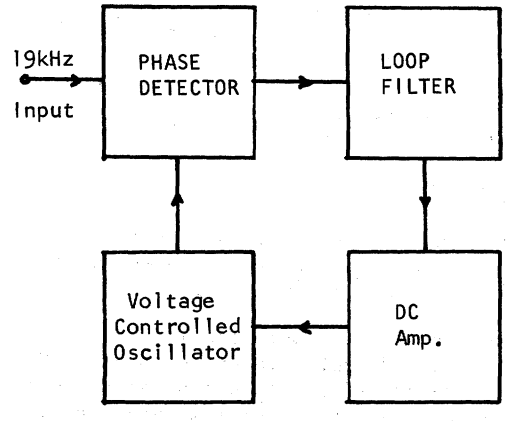

Fig. 2 Basic Phase Locked Loop

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The output of the phase detector is passed through a low pass filter. The filter characteristic, in conjunction with the loop gain, determines the selectivity and the locking characteristics of the PLL as well as the loop stability when in lock.

The D.C. amplifier provides the loop gain required to reduce the worst-case steady state phase error to a value consistent with the separation desired. When in phase lock, the amplified signal is essentially a DC output. This signal is then used as the control voltage for the VCO.

For proper operation, the system should be adjusted so that with no input the DC amplifier is in its active region and the VCO frequency is at or near the expected input frequency (19kHz). When properly implemented, the preceding system will lock onto the 19kHz pilot in the presence of the composite stereo multiplex signal.

THE STEREO DEMODULATOR

In order to adapt the PLL for stereo demodulation, it is necessary to generate a 38kHz phase coherent carrier to demodulate the composite stereo signal. To provide this function, the VCO is expanded into a "Waveform Generation Subsystem" (Fig. III) which consists of a 76kHz VCO and two serially connected binary frequency dividers. The DC input voltage determines the frequency and phase relation of the 19kHz and 38kHz symmetrical square wave outputs to the pilot signal. The 19kHz output is the feedback signal to the phase detector. For recovery of the stereophonic information, the 38kHz output is fed to an audio detector.

The audio detector can be considered as a linear multiplier which multiples two coherent cosine signals to obtain a DC term (audio) and a 2nd harmonic term (noise). The two signals are the 38kHz VCO generated Square Wave and the double sideband surpressed carrier signal containing left minus right information. The resultant is then added to the left plus right signal within the detector. A detailed derivation of the demodulation process is presented later.

THE SYSTEM ELEMENTS

Following the signal path of Fig. I, the first element encountered is the phase detector. An RCA CA 3054 is used (see Fig. IV).

This circuit configuration is currently used as a phase detector in an integrated FM phase lock detector[2] and as a quadrature detector in integrated circuit FM limiter-discriminators[3]. A symmetrical square wave is required as the switching signal input and any arbitrary waveform as the other input. For proper circuit operation, the two inputs are interchangeable.

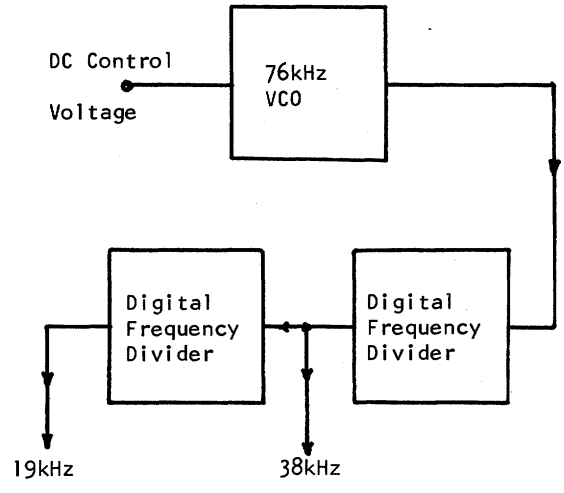

Fig. 3 Waveform Generation Subsystem

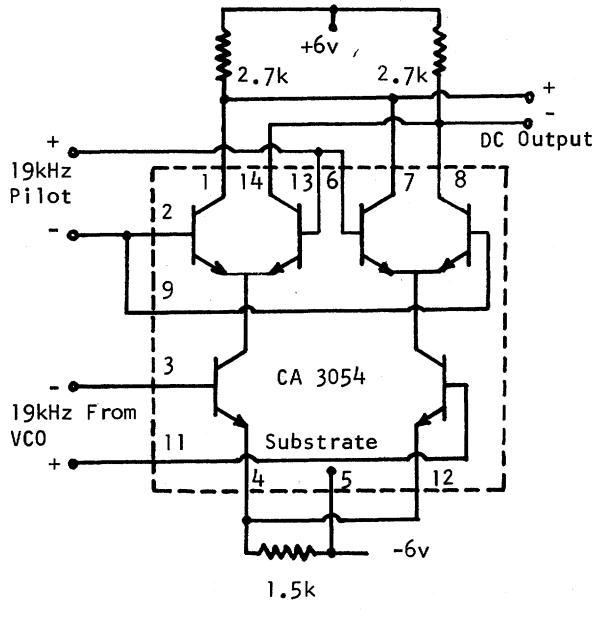

Fig. 4 The Phase Detector

The next system element, the loop filter, appears as a simple one section R/C low pass. Stray capacities within the rest of the system make the simple filter unrealizable.

A standard operational amplifier (Motorola MC1430), differentially connected to minimize the effect of variations in the phase detector's operating point, amplifies the low frequency signal. Proper gain for overall system performance is set by the feedback network. An additional phase shift in the loop is produced by the compensation that the amplifier needs to avoid self oscillation. Therefore, it is necessary to do a stability analysis on the system.

The Waveform Generation Subsystem uses the DC output of the amplifier to control the frequencies of the two symmetrical square wave outputs at 19kHz and 38kHz. Since it is difficult to produce a VCO which guarantees symmetry in its output waveform, the waveforms are generated by the Waveform Generation Subsystem. This subsystem includes a 76kHz VCO which can have an arbitrary output waveform. In the present case, the VCO output is an asymmetrical square wave. A symmetrical 38kHz Waveform is derived from this by a binary frequency divider. The second desired output is produced by another binary frequency divider whose input is obtained from the 38kHz waveform to yield a 19kHz symmetrical waveform.

The 76kHz VCO (Fig. V) is an emmiter coupled astable multivibrator[4] which has a free base to control its frequency. The control voltage applied at the free base also changes the symmetry of the waveform. However, this does not affect the system performance.

Some circuitry is required to interface the VCO with the DC amplifier. It is necessary to reduce the peak to peak output of the DC amplifier to assure that the VCO does not lock into one of its two states and stop oscillating. This is accomplished with a simple voltage divider network.

The two binary frequency dividers used are a standard Motorola MC790P dual J-K Flip Flop. They are powered from the minus 6 volt supply to put their outputs at the proper DC level for driving the lower inputs of the phase detector and audio detector.

The last system element, and possibly the most critical element in the system, is the audio detector (Fig. VI). A circuit gaining acceptance for stereo detection is the synchronous detector used in Motorola's MC1304 integrated circuit[5]. The synchronous audio detector described in the following derivation is similar to that in the MC1304. However, since the switching voltage in this system is at a low DC level (this could be changed) the matrixing can no longer easily be done in the emitter circuit of the lower differential pair. The matrixing in the collectors takes into account that the collector

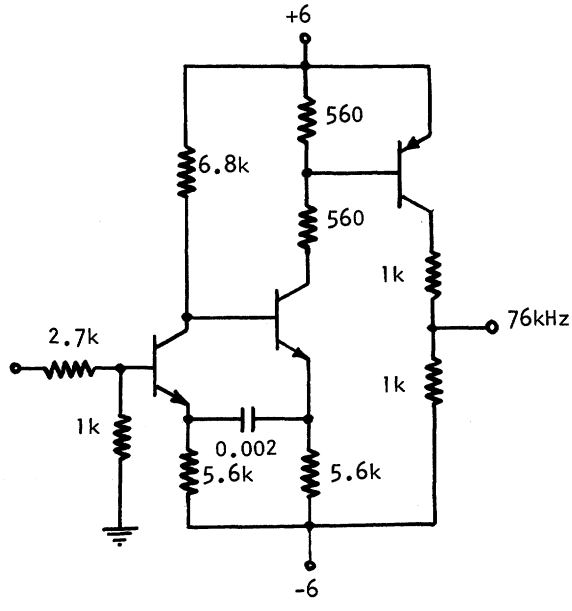

Fig. 5 76 kHz VCO

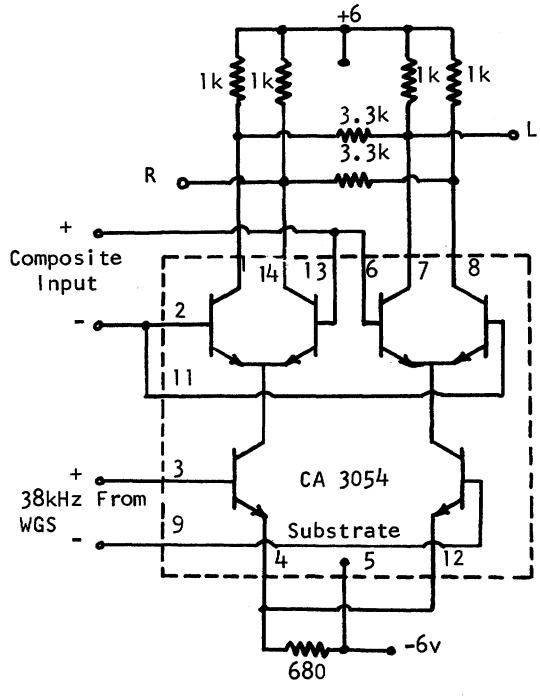

Fig. 6 Audio Detector

AC current in the four upper transistors is as given in Table 1.

CURRENT AT PIN	SWITCHING STATE $V_{PIN3} > V_{PIN\ 11}$	$V_{PIN3} < V_{PIN\ 11}$
1	-(R + KL)	0
14	R + KL	0
8	0	-(L + KR)
7	0	L + KR

TABLE I

The value of K is found by assuming that the audio signals are practically constant with respect to the switching frequency and by normalizing the switching frequency to 1Hz. This gives the composite as a quasi-stationary signal which can be examined graphically (see Fig. VII).

The area A_1 is proportional to the AC output current at pin 14; the area A_2 is proportional to the AC output current at Pin 7.

Therefore:

$$A_1 = \pi L + \pi(R-L)/2 + \frac{(R-L)}{2}\int_0^{\pi} \sin t'dt' \qquad (1)$$

$$= \pi L + (\pi/2)R - (\pi/2)L - \frac{(R-L)}{2}\cos t'\Big|_0^{\pi} \qquad (2)$$

$$= (\pi/2)R + (\pi/2)L - \frac{(R-L)}{2}(-2) \qquad (3)$$

$$= R(\pi/2+1) + L(\pi/2 - 1). \qquad (4)$$

Then normalizing, the output current at pin 14 is:

$$I_{14} = R + \left(\frac{\pi-2}{\pi+2}\right)L \qquad (5)$$

$$= R + kL \qquad (6)$$

$$K = 0.221. \qquad (7)$$

Similarly for the output current at pin 7:

$$I_7 = L + \left(\frac{\pi-2}{\pi+2}\right)R = L + k\,R. \qquad (8)$$

The equivalent circuit for one of the two matrix circuits is shown in Fig. VIII.

Let r_s be the parallel combination of the transistor collector resistance (assumed large), the actual collector resistor, and the load resistance (also assumed large). The equivalent circuit then reduces to the circuit in Fig. IX.

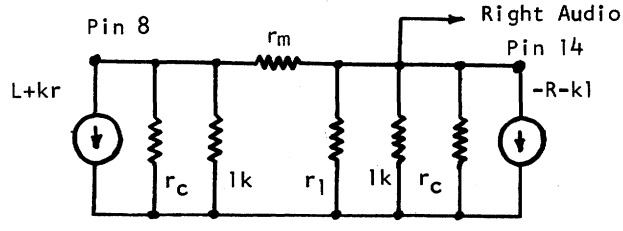

Fig. 8 Equivalent Circuit For One of the Two Matrix Circuits

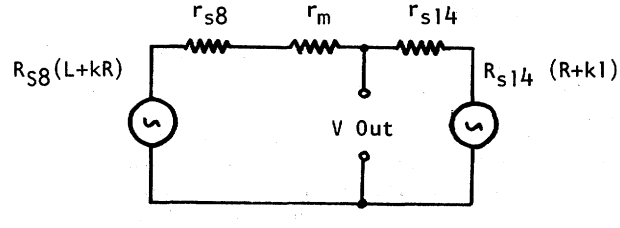

Fig. 9 Resulting Equivalent Circuit

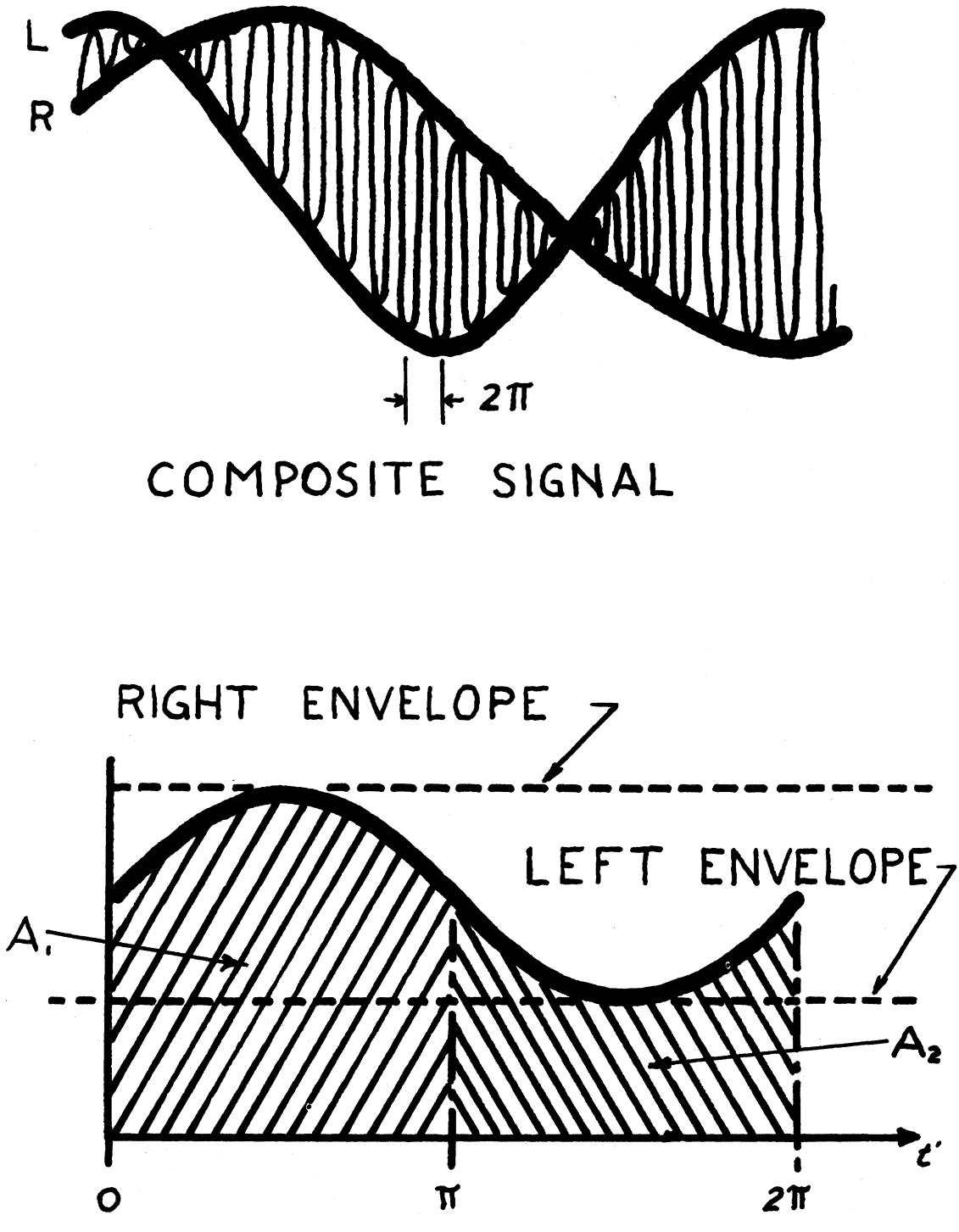

Fig. 7 Graphical Display of Quasi-Stationary Signal

CHART

TEST RESULTS

MEASUREMENT \ DEMODULATOR	DISCRETE			IC VERSION			EXPERIMENTAL I			EXPERIMENTAL II		
	100Hz	1kHz	10kHz	100Hz	1kHz	10kHz	100Hz	1kHz	10kHz	100Hz	1kHz	10kHz
Max. Pilot Level 2% Distortion (mv)		130			70			30			105	
Channel Separation Left (db)												
Pilot level 30 mv		23			37.0			38			38	
50 mv	30	28	9	26	26.0	26	23	34	25	28	37	34
90 mv		29			25.0			20			46	
Channel Separation Right (db)												
pilot level 30 mv		24			42			43			39	
50 mv	29	27		28	27	28	23	32	25	28	39	35
90 mv		20			25			20			38	
Total Harmonic Distortion %												
Pilot level 50 mv Left	1.3	1.5		1.2	1.3		5.4	2.3		0.6	0.3	
Right	1.4	1.1		1.2	1.1		4.5	2.5		0.5	0.4	
(S+N)/N (db)		34			35			25			28	
19kHz % of Noise		90%			50%			-			8%	
38kHz % of Noise		-			5%			70%			54%	
SCA Rejection 60kHz		70db			70db			65db			68db	
67kHz		61db			70db			67db			70db	
74kHz		55db			70db			60db			70db	

$$V_{out} = \frac{r_{s14}\,(R + KL)\,(r_{s8} + r_m)}{r_{s14} + r_{s8} + rm} \qquad (9)$$

$$- \frac{r_{s8}\,(L + KR)\,r_{s14}}{r_{s14} + r_{s8} + r_m}$$

$$= R\,\frac{r_{s14}\,(r_{s8} + r_m) - r_{s8}\,k\,r_{s14}}{r_{s14} + r_{s8} + r_m} \qquad (10)$$

$$+ L\,\frac{r_{s14}\,k\,(r_{s8} + r_m) - r_{s8}\,r_{s14}}{r_{s14} + r_{s8} + r_m}$$

Therefore, for maximum separation:

$$r_{s14}\,K\,(r_{s8} + r_m) - r_{s8}\,r_{s14} = 0\,. \qquad (11)$$

or:

$$r_m = r_{s8}\,\frac{r_{s14}\,(1 - K)}{K\,r_{s14}} \qquad (12)$$

$$= r_{s8}\,\left(\frac{1-k}{k}\right). \qquad (13)$$

For values in the prototype system r_{s8} is approximately 1 kohm.

$$r_m = 10^3\,\left(\frac{1 - 0.221}{0.221}\right) \qquad (14)$$

$$r_m = 3.5 \text{ kohm.} \qquad (15)$$

Since r_{s8} is smaller than 1k, the value used for r_m (3.3k) in the prototype circuit is appropriate.

SYSTEM PERFORMANCE

The Test Chart indicates deficiencies in the initial design with respect to distortion, overload, and noise. The effect of noise jitter at subharmonics of the pilot carrier frequency is not shown.

Non-linearity in the phase detector and audio detector and an unbalance in the audio detector output contribute to these deficiencies. The following circuit modifications were made to improve the results:

1. linearization of the phase detector through feed-back;

2. linearization of the audio detector through feed-back;

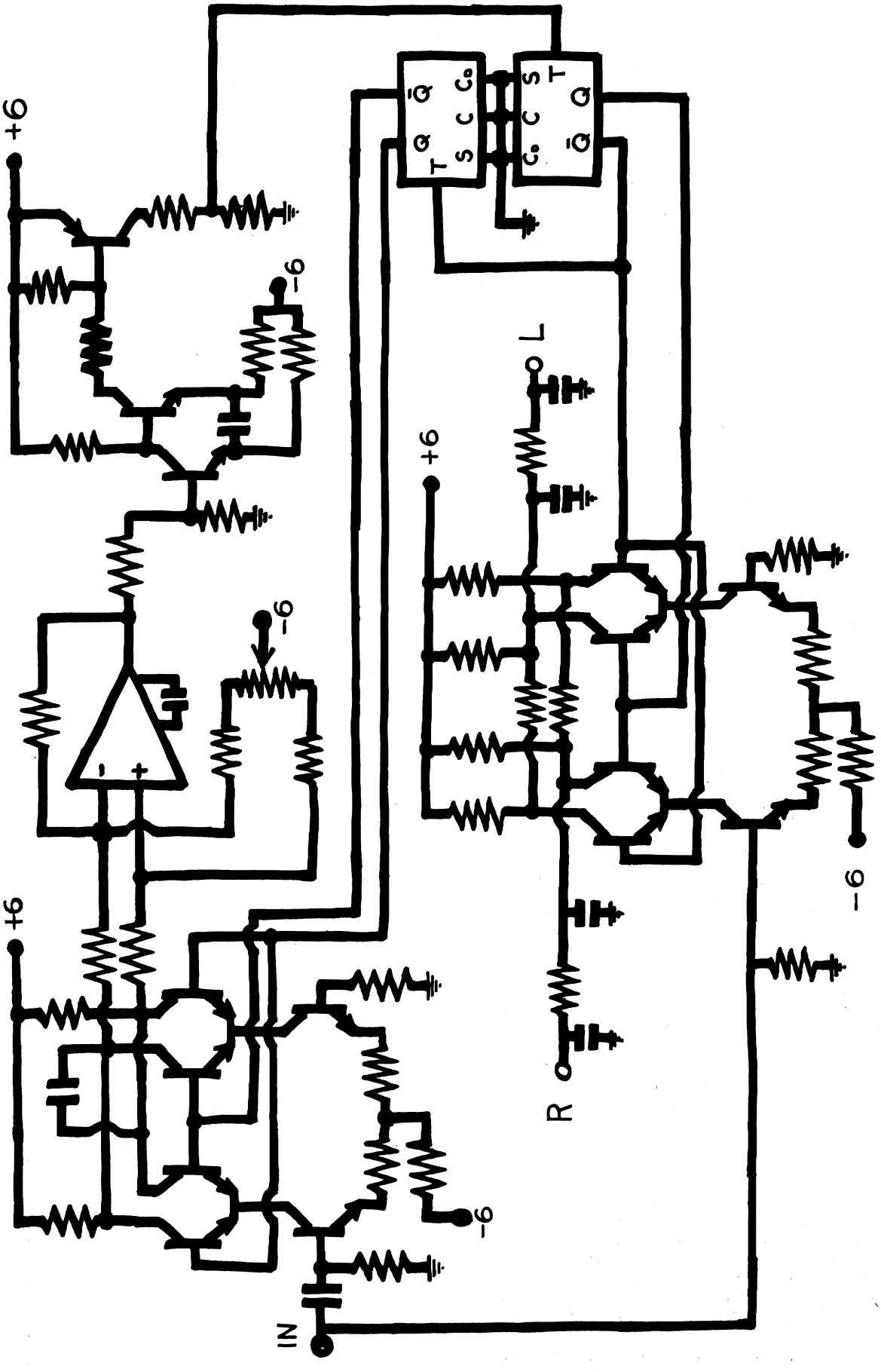

Fig. 10 The PLL FM Stereo Demodulator

3. balancing of the audio detector through parts matching.

Linearization of the phase detector and the audio detector is obtained by incorporating emitter degeneration in the amplifier section of the detectors.

Since the integrated circuits used for these functions (CA 3054) only provide access to the lower transistor emitters, a change in the injection of the 19kHz and 38kHz inputs is necessitated. These inputs are now introduced at the upper transistors of the balanced detector circuits. The tests results are tabulated in column 4 of The Test Chart.

The test results outlined show only a slight improvement in the signal to noise ratio which is still considered unsatisfactory. Since collector matrixing is employed, the noise, which is primarily 38kHz, cannot be appreciably improved. By incorporating matrixing in the emitter, the 38kHz output can be greatly attenuated. The attenuation is then a function of circuit balance.

Significant improvement is obtained in the distortion. It is now at a level below 1%. The overload characteristic measured at a 2% distortion level is improved approximately 10db.

Before the addition of feedback, the 6.3kHz and 9.5kHz audio output frequencies were measured at a 15% distortion level. Linearizing the phase detector reduces this distortion to less than 1% by eliminating phase jitter at these frequencies.

AUTOMATIC STEREO CONTROL

Incorporation of a Quadracorrelator[6] for automatic stereo control is easily implemented by the addition of another phase detector. Its 19kHz injection, 90° out of phase with the original 19kHz output, is obtained from the Waveform Generator through the addition of another frequency divider.

The Quadracorrelator output is a DC signal level proportional to the amount of 19kHz pilot present in the input waveform. It is, therefore, possible to provide an automatic stereo-mono switch or stereo-only performance. AGC control of the PLL may also be obtained from the Quadracorrelator output.

CONCLUSION

The phase locked stereo demodulator described above demonstrates the feasibility of an inductorless circuit. Critical balancing of circuit parts and selection of integrated circuits, which provide close matching of transistor characteristics, are essential. To meet production standards, additional attention is required in the areas of temperature compensation and worst-case analysis of circuit variations.

The circuit and results presented indicate that monolithic circuit techniques provide the necessary matching characteristics for the circuit performance of an inductorless FM Stereo Demodulator to be equivalent to the performance obtained from circuitry using coils.

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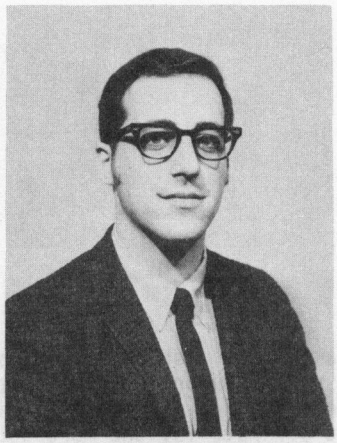
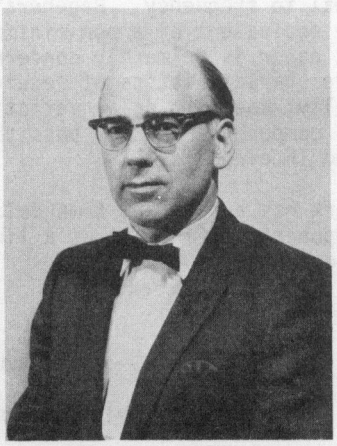
BIOGRAPHIES



Jeffrey N. Denenberg, Senior Engineer at Warwick Electronics, Inc., received his B.S. from Northwestern University in 1966, and his M.S. from Illinois Institute of Technology in 1968. Mr. Denenberg is a member of the I.E.E.E.



William J. Padgett, Manager of Product Research, at Warwick Electronics, Inc. received his B.S. from Illinois Institute of Technology, and the M.B.A. from the University of Chicago, in 1950 and 1968, respectively. Mr. Padgett is a member of the I.E.E.E.