Lecture 12 ; Complementing notes.

Phase Lock Loop (PLL)

In all coherent detection an accurat phase reference is required. Otherwhise it will be difficult or impossible to judge what symbol was transmitted.

Phase synchronization is accomplished by the use of a PLL

A PLL is a feedback loop, the aim of which is to ascertain that the detector locks on the phase of the incoming signal.

It can be schematically described by Fig 1

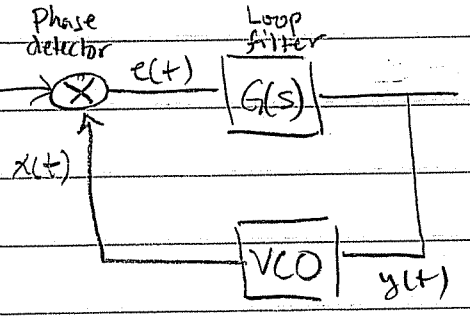


Fig 1

where r(t) is the incoming signal, G(s) is a loop-filter and VCO is a voltage controlled oscillator

For the VCO it holds that:

$y(t) = 0 \Rightarrow$ output frequency $= \omega_0$ (uncontrolled value)

$y(t) > 0 \Rightarrow$ " " " $= \omega_0 + \Delta\omega$

$y(t) < 0 \Rightarrow$ " " " $= \omega_0 - \Delta\omega$

Let the incoming (normalized) signal be

$$r(t) = \cos(\omega_0 t + \theta(t)) \qquad (1)$$

where ω_0 is the (nominal) carrier frequency and $\theta(t)$ is a slowly varying (in comparison to $\omega_0 t$) phase

Furthermore, let the output signal from the VCO be

$$x(t) = 2\sin(\omega_0 t + \hat{\theta}(t)) \qquad (2)$$

where, as in (1), ω_0 represents the (nominal) carrier frequency generated locally and $\hat{\theta}(t)$ is an estimate of the incomin phase $\theta(t)$.

The error signal $e(t)$ can be expressed as

$$e(t) = x(t)r(t) = -2\sin(\omega_0 t + \hat{\theta}(t))\cos(\omega_0 t + \theta(t))$$

$$= -\{\sin(\omega_0 t + \hat{\theta}(t) + \omega_0 t + \theta(t)) + \sin(\omega_0 t + \hat{\theta}(t) - \omega_0 t - \theta(t))\}$$

$$= \sin(\theta(t) - \hat{\theta}(t)) - \sin(2\omega_0 t + \theta(t) + \hat{\theta}(t)) \qquad (3)$$

↑ high frequency component.

Now, if the loop filter $G(s)$ is low pass the input to the VCO will be $\sin(\theta(t) - \hat{\theta}(t))$ which is a function solely of the phase difference.

(For small differences $\sin(\theta(t) - \hat{\theta}(t)) = \theta(t) - \hat{\theta}(t)$.)

When $\hat{\theta}(t) = \theta(t)$ the frequency of the VCO output is ω_0. A change in $\hat{\theta}(t)$ will cause a change in the output frequency. Thus,

$\Delta\omega$ is proportional to the input voltage

$$\Delta\omega(t) = \frac{d}{dt}\left(\hat{\theta}(t)\right) = K y(t)$$

impulse response of G

$$= K\left(e(t) * g(t)\right)$$

$\sin(\theta(t) - \hat{\theta}(t)) \approx \theta(t) - \hat{\theta}(t)$ when $\theta \approx \hat{\theta}$

$$\approx K\left[\left(\theta(t) - \hat{\theta}(t)\right) * g(t)\right] \qquad (4)$$

Using Laplace transforms we can express (4) as

$$s\hat{\theta}(s) = K G(s)\left(\theta(s) - \hat{\theta}(s)\right)$$

$$\left(s + K G(s)\right)\hat{\theta}(s) = K G(s)\,\theta(s)$$

$$\hat{\theta}(s) = \frac{K G(s)}{s + K G(s)}\,\theta(s) \qquad (5)$$

Let $G(s) = \dfrac{B(s)}{s^{k-1} A(s)}$ where $k = 1, 2 \ldots$, $B(0) \neq 0$, $A(0) \neq 0$, and $G(s)$ is strictly proper ($k-1$ free integrators)

We can then express (5) as

$$\hat{\theta}(s) = \frac{K B(s)}{s^k A(s) + K B(s)}\,\theta(s) \qquad (6)$$

The error can now be written as

$$E(s) = \theta(s) - \hat{\theta}(s) = \left(1 - \frac{KB(s)}{s^k A(s) + KB(s)}\right)\theta(s)$$

$$= \frac{s^k A(s) + KB(s) - KB(s)}{s^k A(s) + KB(s)}\,\theta(s) \qquad (7)$$

Now let us investigate how well the PLL will lock on $\theta(t)$ whe $\theta(t)$ varies

Suppose $\theta(t)$ changes as a unit step ie. $\theta(s) = \frac{1}{s}$ $(k=1)$ or a ramp ie $\theta(s) = \frac{1}{s^2}$ $(k=2)$

Then when $t \to \infty$ $e(t) \to 0$ as is evident from

$$\lim_{t\to\infty} e(t) = \lim_{s\to 0} sE(s) = \lim_{s\to 0} \underbrace{\frac{s \cdot s^k A(s)}{s^k A(s) + KB(s)}}_{\to 0} \cdot \frac{1}{s^k} = \frac{0}{KB(0)} \qquad (8)$$

The larger the gain K the faster $e(t)$ will go to zero however, large gains will amplify noise should it be present, so the gain will be a trade-off between phase lock capability and noise sensitivity.

Next, suppose that the carrier frequency of the transmitter is drifting. Then how would the PLL respond? (A change in ω_0 can be caused by doppler shift or by an offset in the transmitter)

Since phase is the integral of frequency the laplace transform is

$$\mathcal{L}\left[\int_{-\infty}^{t} \omega(\tau)\, d\tau\right] = \frac{\omega(s)}{s} \qquad (9)$$

If $\omega(s)$ is a step with amplitude $\Delta\omega$, then

$$\theta(s) = \frac{\Delta\omega}{s^2} \qquad (10)$$

and the steady state error (7) becomes

$$\lim_{t\to\infty} e(t) = \lim_{s\to 0} \frac{s \cdot s^k A(s)}{s^k A(s) + kB(s)} \cdot \frac{\Delta\omega}{s^2}$$

$$= \lim_{s\to 0} \frac{s^k A(s)}{sA(s) + kB(s)} \cdot \frac{\Delta\omega}{s^2} = \frac{\Delta\omega A(0)}{kB(0)} = \frac{\Delta\omega}{kG(0)}$$

$k=1$ (no free integrator) (11)

Here we can see that unless the loop filter $G(s)$ contains a free integrator we will end up with an error signal $e(t) \neq 0$ as $t \to \infty$.

On the other hand, if $G(s)$ does indeed have a free integrator, the we will be able to track step changes in the carrier frequency ω_0 and ramp changes in the phase $\theta(t)$.

Most PLL's is of second order (one free integrator) $= \deg(sA(s)) = 2$. For such PLL's one can proove unconditional stability.

Acquisition

Let us express (4) without the approximation $\theta(t) \simeq \hat{\theta}(t)$. We then obtain

$$\frac{d}{dt}\hat{\theta}(t) = k\left(\sin(\theta(t) - \hat{\theta}(t)) * g(t)\right) \qquad (12)$$

If the loop filter is of first order i.e. $G_2(s) = 1$ we can describe (12) in Fig 2 as

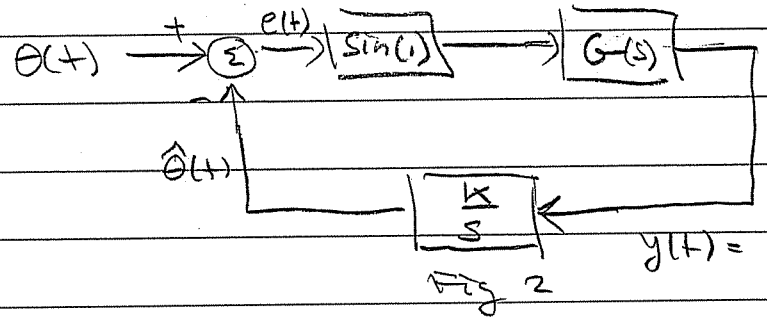


Fig 2

If we set

$$\theta(t) = \omega_i t \qquad \text{and} \qquad G_1(s) = 1$$

and the VCO output phase as

$$\hat{\theta}(t) = \underbrace{\omega_0 t}_{\text{nominal phase}} + \underbrace{\int_0^t k \sin e(t)\,dt}_{\text{phase increment due to the error } e(t)} + \hat{\theta}(0) \qquad (13)$$

The phase error $e(t)$ is then given by

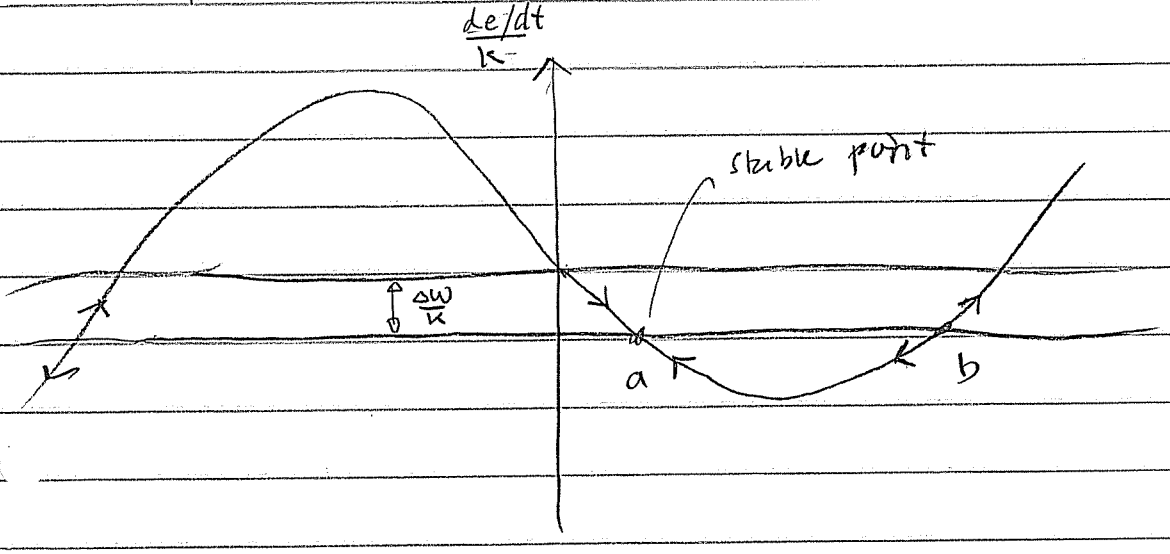
$$e(t) = \theta(t) - \hat{\theta}(t) = \underbrace{(\omega_i - \omega_0)t}_{\text{incoming frequency}} - \int_0^t k \sin(\tau)\,d\tau - \hat{\theta}(0) \qquad (14)$$

Re writing (14) by differentiating both sides and using $\Delta w = w_i - w_o$ gives

$$\frac{de}{dt} = \Delta w - k \sin e(t) \qquad (15)$$

Equation (15) describes the behaviour of a first order PLL

Phase plane analysis reveals that (15) has a stable point and a marginally stable point b



The loop is in lock if $\frac{de}{dt} = 0$ (necessary but not sufficient)

From (15) we note that $\frac{de}{dt} = 0$ cannot be met

Unless $\left|\frac{\Delta w}{k}\right| \leq 1$

$-k \leq \Delta w \leq k$ is called the lock in range of the loop.

A rule of thumb for the loop to lock is $\approx \frac{3}{k}$ seconds. To help the PLL lock sometimes a driving (external) signal is used, eg a voltage ramp on the input to the VCO.