Digital Systems: Computer Architecture

Session for
"Digital Systems: Computers and Communications"
A Fairfield University E-Course
Powered by LearnLinc

Module: Digital Systems (in two parts)

- Texts:
  - "Computers," Capron, Benjamin Cummings, 1996, ISBN 0-8053-0662-5
  - "Telecommunications," Blyth, McGraw-Hill, 1990, ISBN 0-02-680841-2
  - "Understanding Telephone Electronics," Bigelow, Newnes, 1997, ISBN 0-7506-9944
- References:
  - Electronics Tutorial (Thanks to Alex Pounds)
  - Electronics Tutorial (Thanks to Mark Sokos)
- Part 9 – Computers
  - 5 on-line sessions plus one lab
- Part 10 – Digital Communications
  - 5 on-line sessions plus one lab
- Mastery Test part 5 follows this Module

Digital Systems: Topics

- Computer Architecture
  - Memory: ROM, RAM, Cache, Error Checking
  - CPU and Program Control
  - Secondary Storage: Floppy, Hard Drive, CD / DVD
  - I/O (Human: Video, Keyboard, & Pointer)
- Digital I/O: Serial, Parallel, IDE, USB. FireWire, SCSI

Part 9

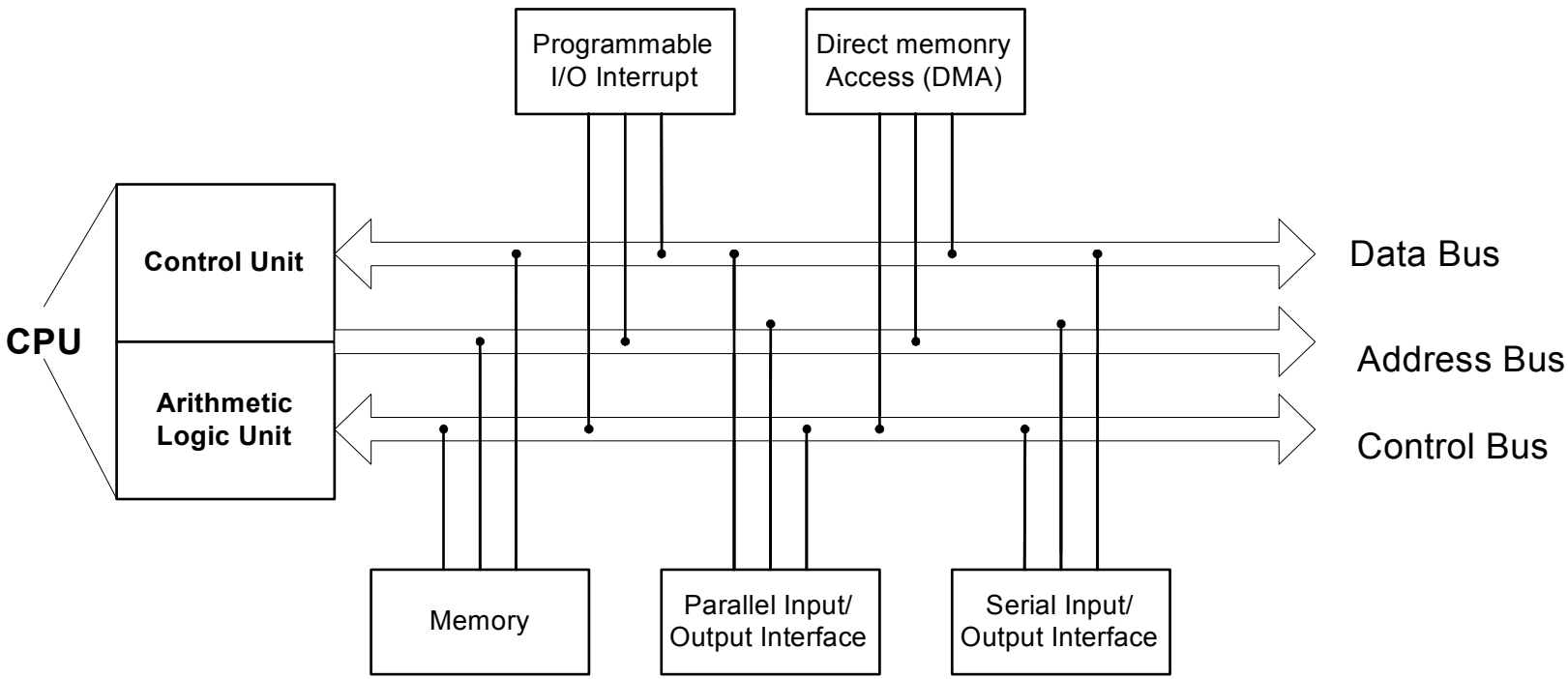
- Serial I/O: RS232
- Modems
  - Telephone: Modulation and Data compression
  - Cable and DSL
- Telephony Digital Transmission
- Packet Transmission
- Fiber Optics: SONET

Part 10

Section 9 Schedule

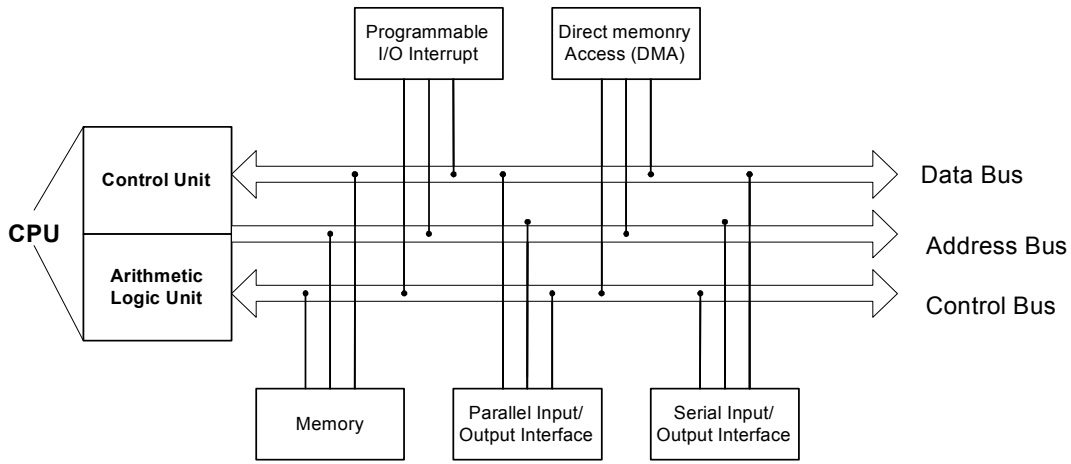
Session 9a (5/26 – Holiday)	**05/21**	**Introduction: Computer Overview**	**Capron: Ch 1; Notes**
Session 9b	05/28	The Central Processing Unit (CPU)	Capron: Ch 2;
Session 9c	06/02	I/O	Capron: Ch 3;
Session 9d	06/04	Data Storage	Capron: Ch 4;
Session 9e	06/09	Digital I/O: Serial, Parallel, IDE, SCSI, USB, and Firewire	Bigelow: pp. 285-288, 301-305; Notes
Session 9f (Lab - 06/14, Sat.) (Quiz 9 due 06/15)	06/11	Review for Quiz 9	
Session 9g (6/18 – no class)	06/16	Quiz Results	

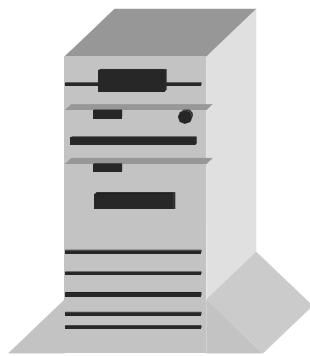
Computer Architecture



Computer Architecture (2)

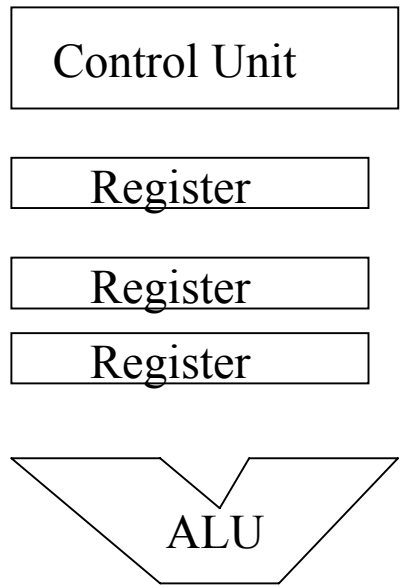
- CPU
  - Control Unit
  - ALU
  - Busses
    - Data
    - Address
    - Control (buss operation)
- Memory
- Interrupts
- DMA
- Parallel and Serial I/O





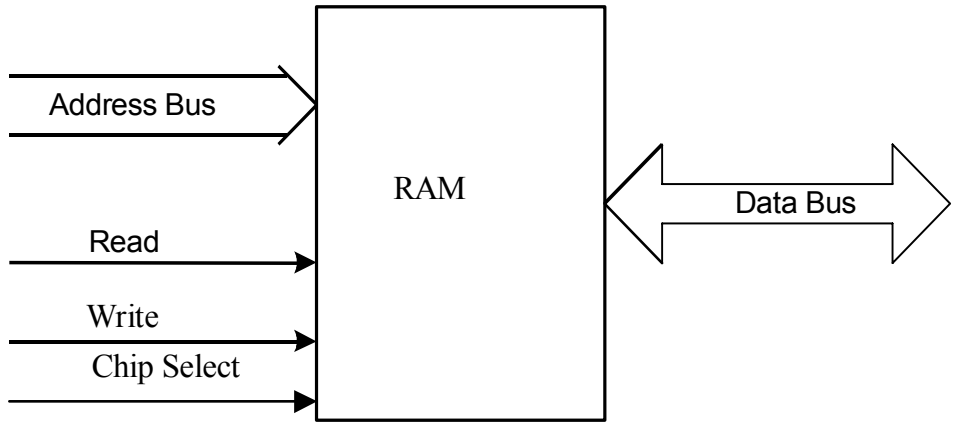
Central Processing Unit

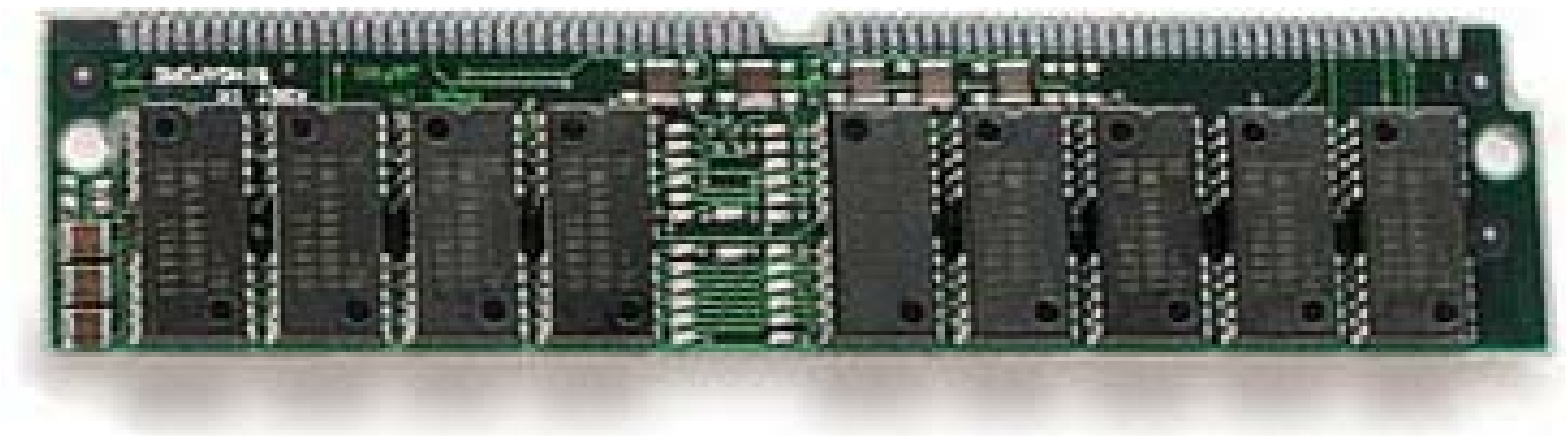
- Control Unit
  - Sequential control of operations
  - Program Memory determines sequence
- Register: Fast temporary Data storage
- Arithmetic Logic Unit (ALU)
  - Fixed Point
    - 18.75 Decimal
    - 0010010.1100 12-bit Binary (1 sign bit)
  - Floating Point
    - $0.1875*10^{2}$ Decimal
    - $00001100*2^{0010}$ 12-bit Binary (2 sign bits)



Memory

- DRAM SIMM
  - Dynamic RAM
    - Low Power
    - Refresh
  - Single Inline Multi-Chip Module





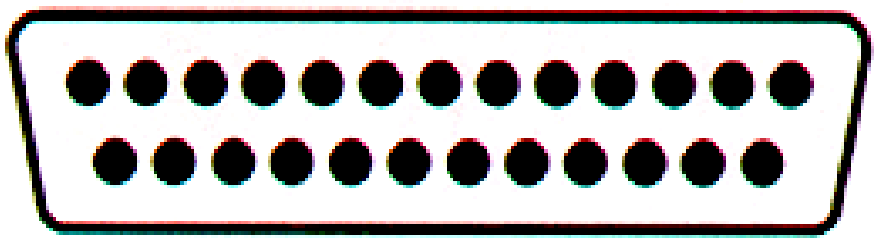
Interrupts

- Allows software multi-tasking
- Operating system (Windows, Linux, etc.)
  - Looks for interrupt flag
    - Hardware:
      - Peripheral
      - Timing
    - Software
  - Sets aside current task
    - Saves all “State” information for the current task
    - Restores “State” information for new task and runs it for a limited time

Direct Memory Access (DMA)

- Fast add-in card and memory communications
  - Hard Disk Storage
  - High Speed I/O
- Bypasses CPU
  - CPU defines block transfer
  - DMA controller manages transfer

Serial and Parallel I/O



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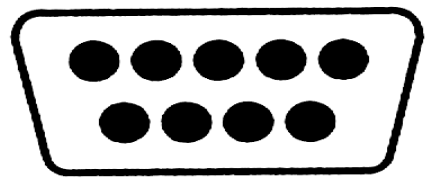

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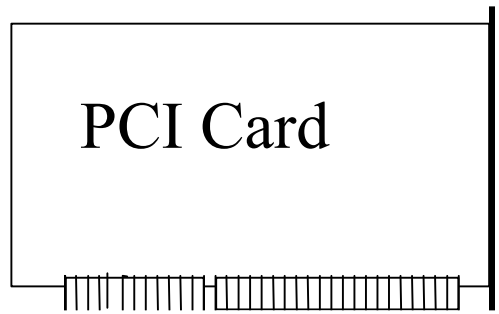
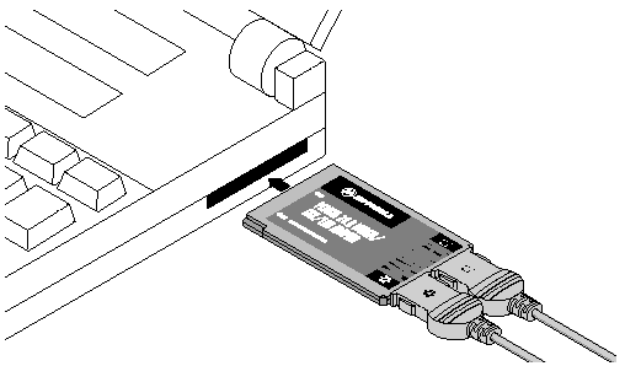
Centronics 36pin male

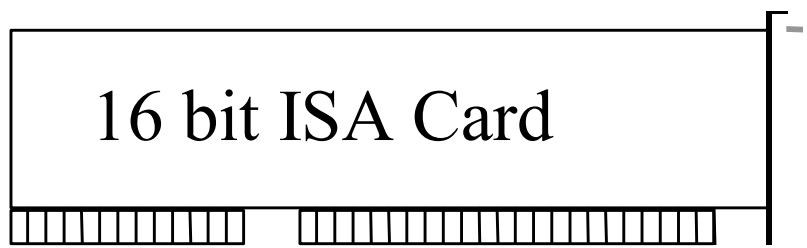
Centronics 34 pin female

PC Add-In Hardware: Peripherals

- ISA: Industry Standard Architecture (old)
  - Original IBM PC (Cloned)
  - PS2 (32-bit IBM)
  - VESA & EISA (Clone 32-bit)
- PCI: PC Interface (Current Standard)
- PCMCIA (PC Card: Portable Standard)

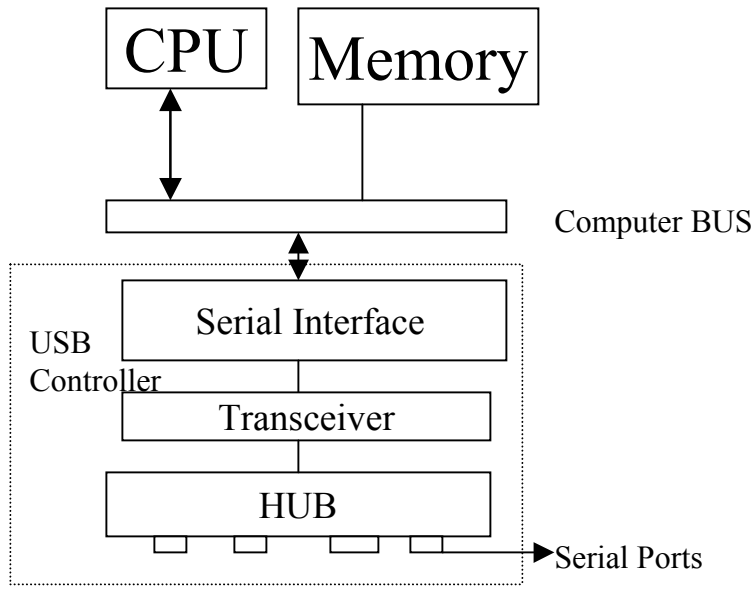






Universal Serial Bus

- New Standard Peripheral Connection System
  - Serial Data
    - USB 1: 12 Mbit/Sec
    - USB 2: 400 Mbit/sec
  - Tree Topology (Hubs)
  - Limited DC Power to USB Peripherals (Use Auxiliary Bricks)



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