Digital Systems: Central Processing Unit (CPU)

Session for
"Digital Systems: Computers and Communications"
A Fairfield University E-Course
Powered by LearnLinc

Module: Digital Systems (in two parts)

- Texts:
  - "Computers," Capron, Benjamin Cummings, 1996, ISBN 0-8053-0662-5
  - "Telecommunications," Blyth, McGraw-Hill, 1990, ISBN 0-02-680841-2
  - "Understanding Telephone Electronics," Bigelow, Newnes, 1997, ISBN 0-7506-9944
- References:
  - Electronics Tutorial (Thanks to Alex Pounds)
  - Electronics Tutorial (Thanks to Mark Sokos)
- Part 9 – Computers
  - 5 on-line sessions plus one lab
- Part 10 – Digital Communications
  - 5 on-line sessions plus one lab
- Mastery Test part 5 follows this Module

Digital Systems: Topics

- Computer Architecture
  - Memory: ROM, RAM, Cache, Error Checking
  - CPU and Program Control
  - Secondary Storage: Floppy, Hard Drive, CD / DVD
  - I/O (Human: Video, Keyboard, & Pointer)
- Digital I/O: Serial, Parallel, IDE, USB. FireWire, SCSI

Part 9

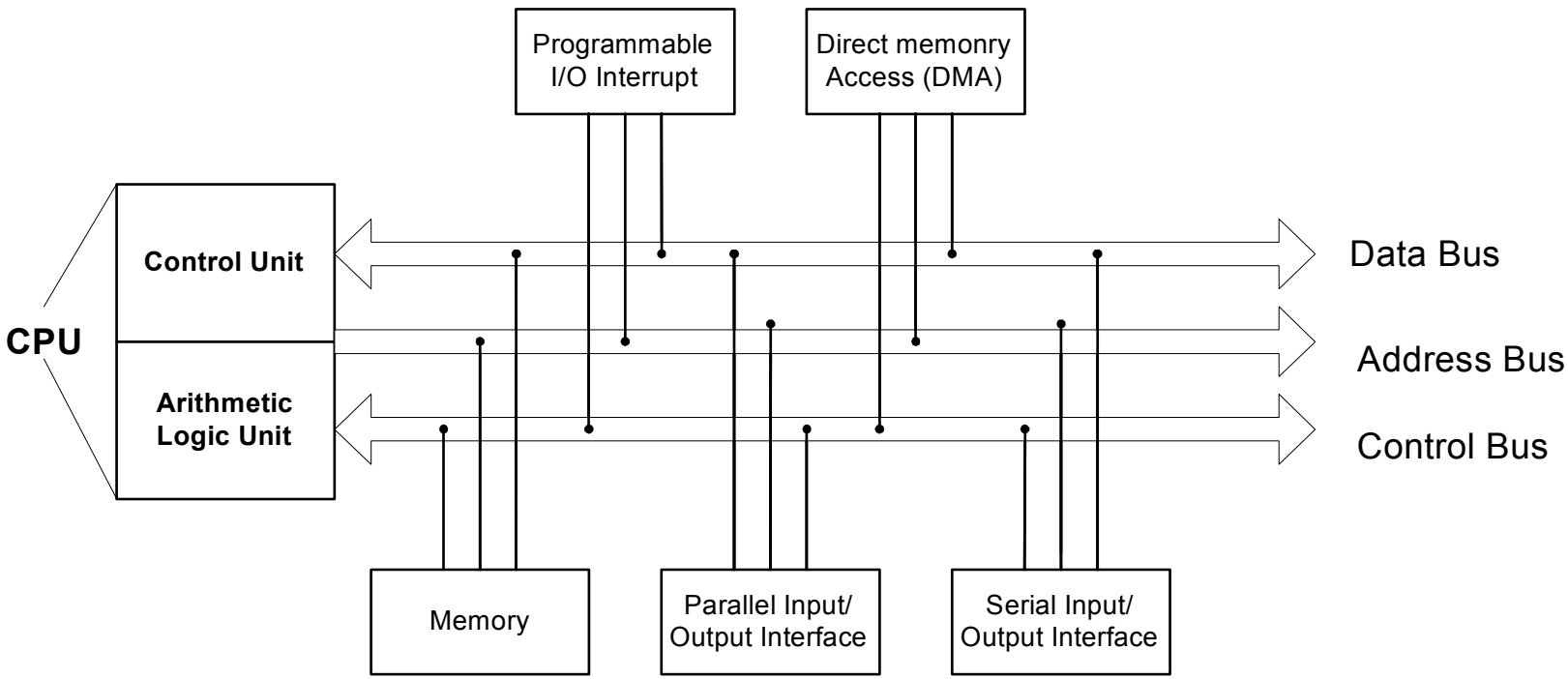
- Serial I/O: RS232
- Modems
  - Telephone: Modulation and Data compression
  - Cable and DSL
- Telephony Digital Transmission
- Packet Transmission
- Fiber Optics: SONET

Part 10

Section 9 Schedule

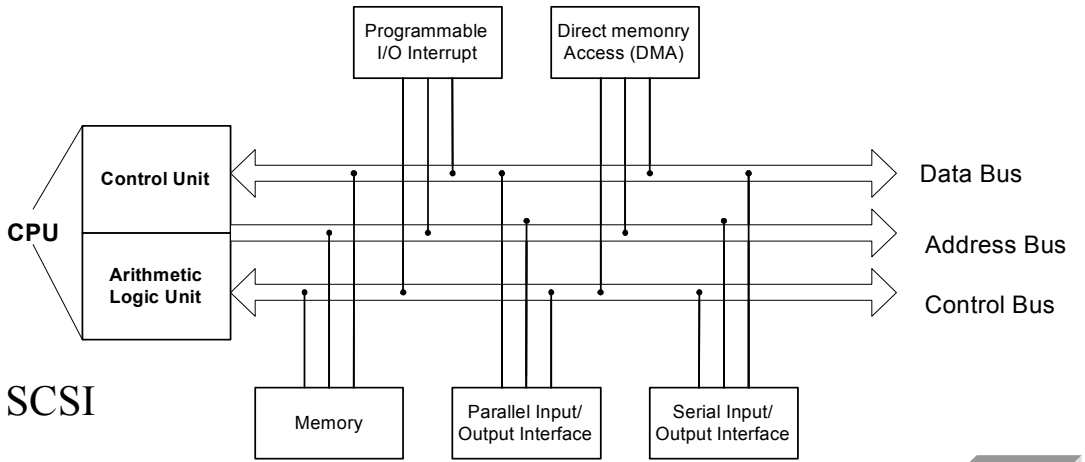
Session 9a (5/26 – Holiday)	05/21	Introduction: Computer Overview	Capron: Ch 1; Notes
Session 9b	**05/28**	**The CPU (Central Processing Unit)**	**Capron: Ch 2;**
Session 9c	06/02	I/O	Capron: Ch 3;
Session 9d	06/04	Data Storage	Capron: Ch 4;
Session 9e	06/09	Digital I/O: Serial, Parallel, IDE, SCSI, USB, and Firewire	Bigelow: pp. 285-288, 301-305; Notes
Session 9f (Lab - 06/14, Sat.) (Quiz 9 due 06/15)	06/11	Review for Quiz 9	
Session 9g (6/18 – no class)	06/16	Quiz Results	

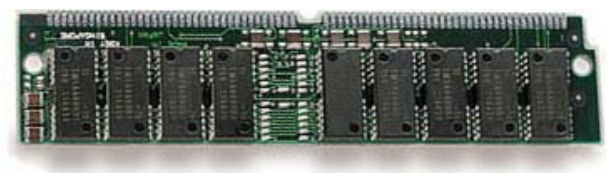
Computer Architecture Review

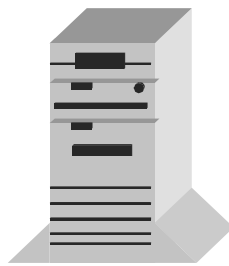


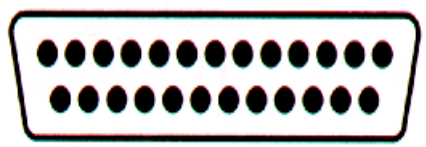
Computer Architecture Review (2)

- CPU
  - Control Unit
  - ALU
  - Busses:
    - Multiple:
      Memory, PCI, SCSI
    - Structure:
      - Data
      - Address
      - Control (buss operation)
- Memory:
  RAM, ROM, Cache, & Secondary
- Interrupts: HW & SW
- DMA: Fast data transfer
- Parallel and Serial I/O









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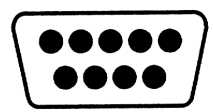

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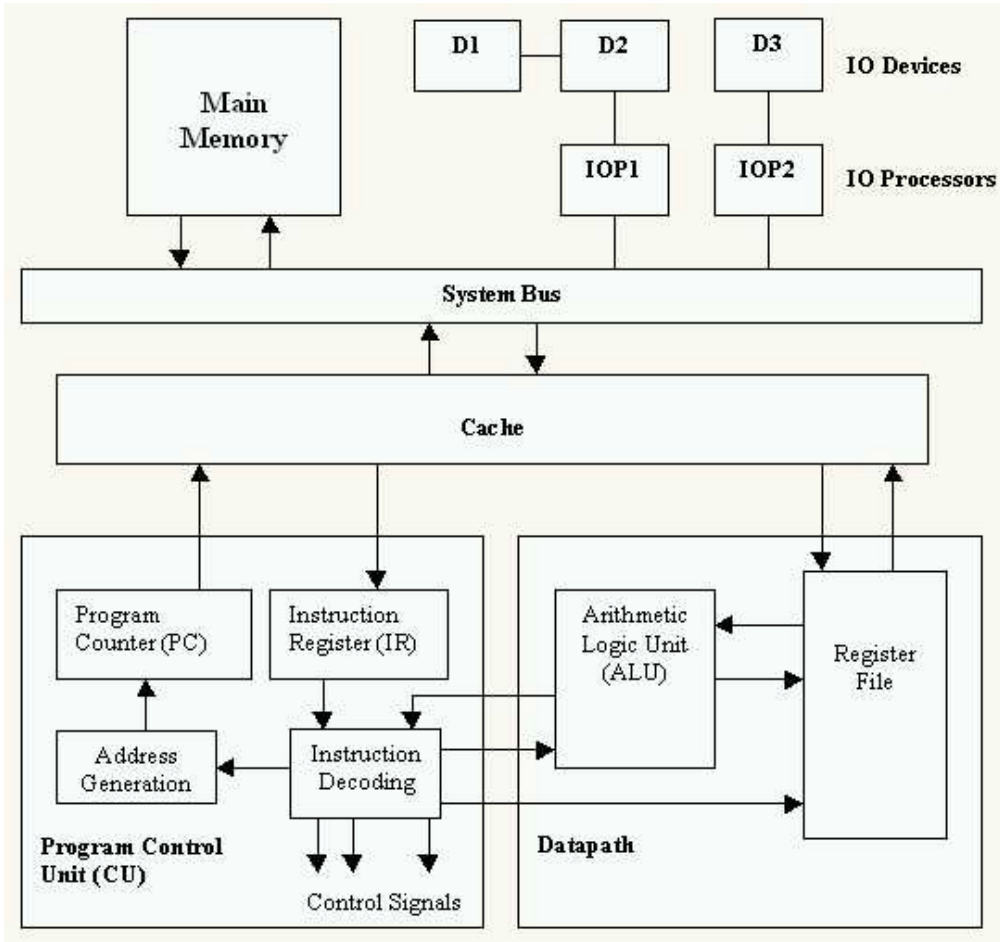
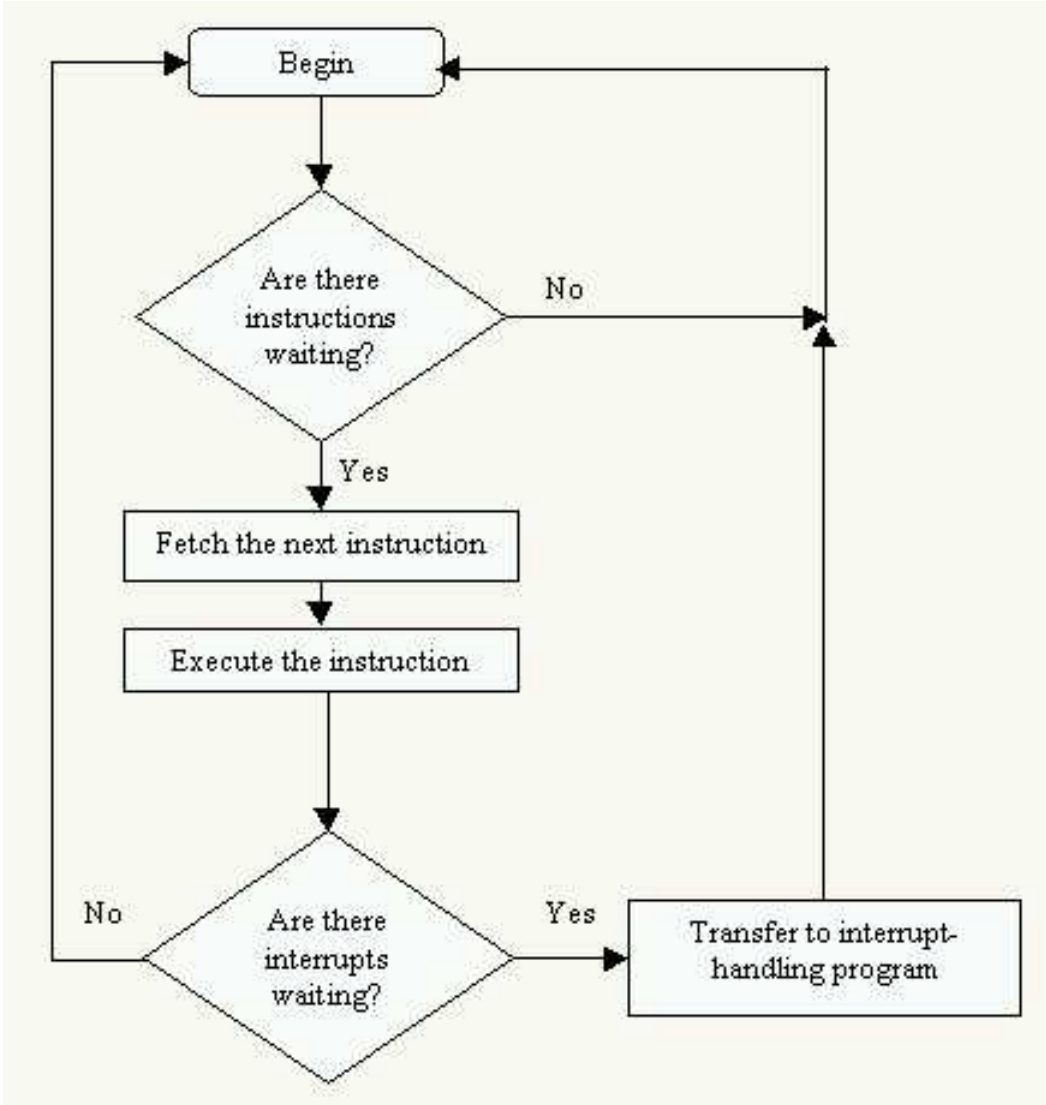
Central Processing Unit (CPU) or Micro Processing Unit (MPU)

- Control Unit
  - Sequential operation control
  - Program Memory: determines operation sequence
- Register: Fast temporary storage
- ALU: Arithmetic Logic Unit
  - Fixed Point
  - Floating Point
  - Boolean Logic



Control Unit: Sequential control of operations

- The part of a CPU responsible for performing the machine cycle - fetch, decode, execute, store
- Fetches instructions from main memory and determines (decodes) their "type"
- Instruction "type" determines operation
  - Control Unit sequences the logic to perform the operation (execution)
  - Uses the "Registers" to accomplish the task
- Each "type" is an "OpCode" with parameters

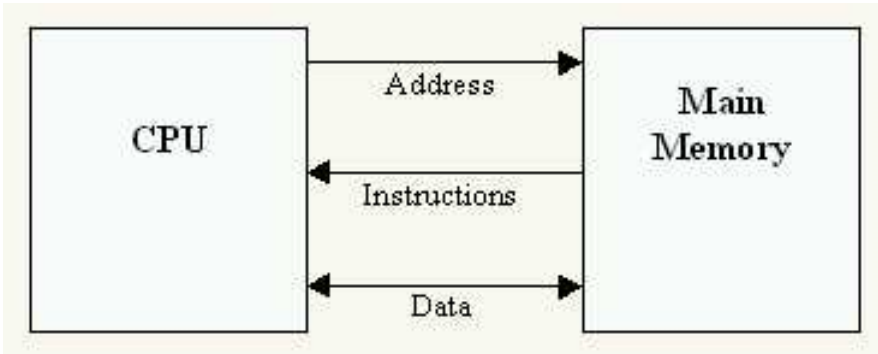


Typical CPU Op Codes & Operands

ADC	add with carry (AC + DR ⇒ AC)	LD adr	load AC from memory
ADD DR	add (AC + DR ⇒ AC)	LSR	one-bit shift right (AC)
AND	bit-wise logical AND (AC AND DR ⇒ AC)	NEG	two's complement negate (AC)
ASR	one-bit arithmetic shift right (divide AC by 2)	OR	bit-wise logical OR of AC and DR
BZ adr	Jump to instruction at adr if AC = 0	OUT #	output AC to port #
IN adr	input from port	SBC	subtract with borrow (AC – DR ⇒ AC)
JEQ adr	jump to adr if DR = AC	SL	one-bit shift left
JGE adr	jump to adr if DR ≥ AC	ST adr	store AC in memory
JMP adr	Jump to adr	SUB	Subtract (AC – DR ⇒ AC)

Typical Registers

AC	Accumulator	stores the input or output (result) operand
DR(n)	Data register	stores a data word
PC	Program Counter	stores the instruction address
IR	Instruction Register	stores the instruction OpCode



Programming

- Machine Language:
  - Object code: specific to Hardware
  - Ones and Zeros: not for human consumption
- Assembly (programmer must have detailed knowledge of the hardware)
  - Human readable
  - Translated to “relocatable” machine code
  - Linked to produce binary “Object code”
- High-Level
  - Compiler: “C”, “C++”, Fortran, Cobol
    - Compiler “Parses” “source code” into assembly
    - Assembled and “linked” to produce object code
    - About 3 times slower than well written assembly
  - Interpreter: Basic, Java (easies to get working)
    - Source code is tokenized (sometimes miscalled compiling)
    - The “interpreter” then translates the program steps into machine code on-the-fly.
    - About 3 times slower than true compiled programs

ALU (Arithmetic Logic Unit)

- Fixed Point
  - Decimal arithmetic: 18.75
  - Binary arithmetic: **0**0010010.1100 12-bit (1 sign bit)
    - Bits to the left of the "Binary Point"; Powers of 2
    - Bits to the right of the "Binary Point"; Powers of ½
    - -255 to 255 (7 significant bits for magnitudes above ± 4)
- Floating Point (scientific notation)
  - $0.1875*10^2$ decimal floating point
  - **0.**001100 * $2^{\mathbf{0}00010}$ 12-bit Binary (2 sign bits)
    $(1/8 + 1/16)*2^2$
  - 7 significant bits; $\pm 2^{-15}$ (1/32768) to $\pm 2^{+15}$ (32768)

PC Boot Sequence

- ROM-based routines
  - Power-on System Test (POST)
  - Bootstrap: Go to Disk (boot sector) to start the OS
  - Basic Input Output Sequences (BIOS)
    - Hardware specific operations
    - Used by the Operating system
      (in MSDOS used directly by application software)
- Operating System (OS): Windows, Linux, Mac (OSX) etc.
  - Provides environment for applications (API)
  - Resource Sharing: Multitasking, Virtual Memory

Memory Hierarchy

- Registers: directly used by CPU
- Cache: Fast, local, temporary storage
  - L1: same speed as the CPU; small size (only 16 Kbytes in old PCs)
  - L2: somewhat slower; somewhat larger (Not often present)
- Core Memory: Originally magnetic cores (toroids)
  - Dynamic silicon RAM
    - Fast Page Mode (FPM) DRAM: old – early 1980s; PC XT; 8088
      - 70 ns; 36 pin SIMM : byte-wide data or 72 pin: wider data path
    - EDO DRAM: "486" (60 ns; 72 pin SIMM or DIMM)
    - SDRAM (DDR): Pentium (10ns to 5 ns-pc3200)
- Secondary Storage: Disk (cache memory in fast disks; 1-2 Mbytes)
  - Access time (Read/Write head speed)
  - Write speed (rotation rate; 5000, 7500, 10k rpm)

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